THE VIRTUOUS CIRCLES OF THE RTOS

HOW TO SUPPORT AND BOOST TECHNOLOGY DEVELOPMENTS FROM MATERIALS TO INTEGRATION

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OUTLINE

• RTO ecosystem
• 3 focuses on RTO efficiency parameters
  • Fab capabilities
  • Technology development
    • CMP program
    • DSA patterning
  • Fab performances
• Conclusions
WHAT IS A RTO?

• **Definition**

  • RTOs are non-profit organizations with public missions to support society providing
    • Research and development, technology and innovation services to enterprises, governments and other clients…” (EURAB 2005).
    • Their mission is to help companies move “one step beyond” their existing capabilities
    • Reduce the risks associated with innovation for a faster rate of economic development

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**RTO position**

- **Pre-industrialization**
  - Prototyping
    - Proof of concept and prototyping capability taking into account the partner mass production constraints to ensure fast technology transfer and reduced time to market.

- **Advanced Research**

- **Industrial Partnership**

- **Mass market / Growth**
  - Smooth transfer to go mass market. Long term bilateral partnership with year-over-year results and customer satisfaction.
CEA-LETI RTO KEY FIGURES

“3rd Innovative Public Research Organization Worldwide” 2012 -2020

- Since 1967
- 2,000 people

Patents:
- > 3,000 in portfolio
- 40% under license agreement

Startups:
- 68 created for 20 years (75% in activity)

Cleanrooms:
- 500 state-of-the-art equipment in 200 et 300 m²
- 10 000 square meters cleanroom

Budget:
- 315 M€
- 85% from R&D contracts
UNIQUE ECOSYSTEM: 3 VALLEYS

Microelectronics Valley
6,000 direct jobs

Display Valley
500 jobs expected in 2024

Imager Valley
1,500 direct jobs
OUTLINE

• RTO ecosystem

3 aspects of RTO efficiency parameters

• Fab capabilities
• Technology developments
  • CMP program
  • DSA patterning
• Fab performances

• Conclusions
FOCUS 1 – Manufacturing capability

Technology developments

Performances

Manufacturing capabilities
LETI TECHNOLOGY PLATFORM CAPABILITIES

- 300mm & 200mm Si components Platforms
  - ~270@200mm equipments
  - ~105@300mm equipments
  - 5600 square meters Cleanroom - ISO3-5
  - 24/7 operations

- 200mm MEMS Platform
  - ~130@200 mm equipments
  - 2200 square meters - ISO 4-5
  - 24/7 operations

- Substrates <200 mm, III-V and II-VI Platform
  - ~230 @ various diameter equipments
  - 1000+1000 square meters - ISO 4-5
  - 1shift/day

- Nano-CHARACTERIZATION Platform
  - ~ 40 huge equipments
  - 2200 square meters
  - 8 centers of competences

NEW PHOTONICS PLATFORM IN 2017

Concentration of Means to Address Large Photonics Challenges Closely with the Silicon Platform
MATURE & UP-TO-DATE PLATFORMS

- FC300 DtW High Speed
- Laser Annealing
- Low Temp Epi MOCVD
- Direct hybrid bonding
- Dielectric Contact Etching
- PCM Endura
- 193i Scanner
FOCUS 2 – Technology innovation

Technology developments

Performances

Manufacturing capabilities
Fab-like equipments
Large process versatility
TECHNOLOGY DEVELOPMENT  FUELS INNOVATION

ARCHITECTURES
- RF, Neural Network, Smart Sensors, Actuators, LiFi …

MATERIALS
- SOI, SiC, GAN, III-V, GST, polymer, slurry …

PROCESS INTEGRATION
- Module and process flow Patterning – deposition - surfacing

PACKAGING
- Pixel Array, Memories LNA, PA, PMUT, Photo-Acoustic…

COMPONENTS & DEVICES
- LED, T-MOS RF Switch, MEMS, NVM-RAM, TSV …

MASTERING THE DEVELOPMENT OF INDUSTRIAL TECHNOLOGY SOLUTIONS
From materials to device
CLOSE PARTNERSHIPS WITH KEY SUPPLIERS

Deposition
- Applied Materials
- Solmates
- Avanti

Patterning
- Lam Research
- ASML
- ASM International
- SCREEN
- TEL
- JSR Corporation

Surfacing
- Ebara
- Applied Materials
- Entegris
- EV Group
- Soitec
- SCREEN
- NAGASE Group

Metro/Charac
- Unity
- KLA
- Rigaku
CMP CHALLENGE
INCREASE SLURRY LIFETIME W/O YIELD IMPACT ON DEVICE

Study & understand filtration efficiency

- big particles filtration to prevent scratches defects
- Maintain slurry optimal properties by optimizing natural particle size distribution
  - Removal rate
  - Planarization efficiency
  - Selectivity

New generation slurries for 10 nm node or less
Colloidal SiO2 based particles slurries
Ceria based slurries

Particle agglomerates, gels, particles generated inside the distribution system and inside the polisher

Incoming slurry
Filter
Outgoing slurry
OPTIMIZE CMP PROCESS FLOW & EFFICIENCY

1. **Filter selection optimization on test Bench**
   Selection of key monitoring parameters for slurry/filter couples

2. **Test best filters set up on CMP tool**
   Verify CMP process performances on blanket and patterned lot wafers

3. **Filter life time optimization**
   Quantify efficiency gain and perform optimization loops

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**FILTER TEST BENCH**

- Acusizer
- Filter

**Optimisation Loops**

**CMP Tool**

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**3 YEARS PROGRAM**

**CMP PROCESS flow CHAIN OPTIMIZATION**
CLOSE PARTNERSHIPS WITH KEY SUPPLIERS

Deposition
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- Solmates
- aveni

Patterning
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- ASML
- EVG
- SCREEN
- TEL
- JSR Corporation

Surfacing
- Ebara
- Applied Materials
- Entegris
- Soitec
- SCREEN
- Nagase Chemtex

Metro/Charac
- Unity
- KLA
- Rigaku
- Bruker
- Applied Materials
DIRECTED SELF ASSEMBLY CONCEPT

BCP + GUIDE

High chi – L0=18nm

DSA chemoepitaxy with 22nm period PS-b-PMMA
IMB-CNMI & Leti collaboration
L. Evangelio et al., talk at 2nd DSA Symposium,
Grenoble (France), October 2016

DSA gaphepitaxy with 38nm period PS-b-PMMA
G. Claveau et al., J. Micro/Nanolith. MEMS
MOEMS 15(3), 031604 (2016)
Grapho-epitaxy demonstration
N10 demonstration capability
2012-2018

Contact hole shrink and doubling

Line/Space patterning

Nanowire

Partnership framework

Industrial
- ARKEMA
- IDEAL

Institutional
- Horizon 2020
- COLISA – Ion4SET
- PLACYD – MADEin4
- bpifrance
- REX-7
**DSA MATERIAL PORTFOLIO**

**HighX** (L₀<20nm)
- Mandatory for sub N5 L&S

**L22** (PS-b-PMMA)
- Contact: Suitable down to N5
- L&S: scalable down to N7
- Other application: sensors surface

**L38** (PS-b-PMMA)
- 1st Gen DSA materials
- Main application: contact/via
- Other application: sensors surface

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BLOCK COPOLYMERS FOR NON-CMOS APPLICATION

Low-cost surface structuration for MEMS sensor

SiGe Epi growth template

Si nanopillars
Inverted PS-\textit{b}-PMMA matrix
\( h = 70 \text{ nm}, \varnothing 15 \text{ nm} \)
DSA FOR CMOS APPLICATIONS

1st Gen DSA materials
- Main application: contact/via
- Other application: sensors/surface

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Process ecosystem

Process Development
DSA DEVELOPMENTS

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**Process Development**

**Process ecosystem**
ADVANCED METROLOGY

Advanced CD-SEM

Low energy (300 V), low # frames to prevent resist shrink
Large grab for local statistics
Tilted beam metrology

Scatterometry

3D metrology at every process step

\[ \text{TMU} = 0.36 \text{ nm} \ (48 \text{ pt.}) \]

CD-SAXS/GISAXS

→ Reference for 3D metrology
→ LWR : Extraction of PSD

\[ q_x (\text{nm}^{-1}) \]
\[ q_z (\text{nm}^{-1}) \]

See presentation Freychet et al. SPIE AL 2020 (parallel session)

Critical-dimension grazing-incidence small angle X-Ray scattering: applications and development
SOFTWARE SUITS FOR MATERIALS & PROCESS EVALUATION

Free surface defect analysis

Line end assembly for lamellar BCP

Grain boundaries for cylindrical BCP

Directed Self-Assembly

Def Line/space patterns

CD, Hole open yield & Pattern placement error
LWR EXTRACTION
POWER SPECTRAL DENSITY (PSD)

• **Unbiased** roughness metrology is necessary
  • Frequential breakdown to correct for CD-SEM noise floor bias

• Unique reference measurement method by synchrotron radiation (CD-SAXS)
  • **Measure of lower frequencies**
  • Lower noise floor at high frequencies

• Line width roughness on fingerprint samples for BCP material evaluation
  • Algorithm development shared with photonic circuit applications


FIRST DEFECT INSPECTION WORK
L&S

• Defect inspection & review:
  • Applied Materials UVision 8
  • Applied Materials SEMVision G7E

• Determination of pixel size, polarization and laser power adapted to PS lines (PMMA removed)
SMALLER DEFECTS EXTRACTION CPAPABILITY

- Reduction of scan area to one shrunk array box
- Adaptation of pixel size and polarization mode

T19S893-P06 Slot 06
Defect Count : 18580

T19S893-P17 Slot 16
Defect Count : 11512

T19S893-P07 Slot 25
Defect Count : 16927
The higher resolution mode allows for finding:

- Large assembly defects
- Smaller dislocations (e.g. 3)

*Without etching PS into TiN substrate*
DSA DEVELOPMENTS

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Process Development
Process ecosystem
<table>
<thead>
<tr>
<th>SiARC/SOC</th>
<th>SiARC/SOC</th>
<th>Silicon Oxide</th>
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<tbody>
<tr>
<td><strong>Organic template</strong></td>
<td><strong>Embedded NL</strong></td>
<td><strong>Inorganic template</strong></td>
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<td><strong>Guide template:</strong></td>
<td><strong>Guiding template:</strong></td>
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<td><strong>DSA:</strong></td>
<td><strong>DSA:</strong></td>
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<tr>
<td>$\text{CD} = 17.2\ \text{nm}$</td>
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<td>$\text{HOY} = 100%$</td>
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<tr>
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<td>Rework: NO</td>
<td>Rework: OK</td>
</tr>
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</table>

**Several process options available for Contact hole integration**
ADVANCED L&S PROCESS : “ACE” CONCEPT

1st part: SADP PROCESS

Lithography
Mandrel etch
Spacer deposition
Spacer etch
Mandrel pull

2nd part: DSA PROCESS ACE

Deposition of neutral layer
Spacer removal by wet etching
Selective grafting of guiding material
BCP self-assembly
ACE PROCESS ADVANTAGES

• Reduce multi-patterning scheme for SAxP strategy
• Support EUV insertion
  ▪ Allow low Multiplication factors
  ▪ Mitigate LER
  ▪ Relax masks issues for clear field levels

Lithography guide period (nm)

<table>
<thead>
<tr>
<th>Process</th>
<th>BCP $L_0$ (nm)</th>
<th>MF2</th>
<th>MF3</th>
<th>MF4</th>
<th>MF5</th>
<th>CD guide (nm)</th>
</tr>
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<tbody>
<tr>
<td>LiNe &amp; SMART</td>
<td>30</td>
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<td>90</td>
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<td>84</td>
<td>112</td>
<td>140</td>
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</tr>
</tbody>
</table>

193i  
EUV  

Difficulty
SPACER PATTERNING RESULTS

500 nm
DSA of $L_0 = 31.5$ nm, MF = (2,2)

*(RESULT PRESENTED AT SPIE ADV LITHO 2020)*

At least 10 $\mu$m x 10 $\mu$m without defects
First results of DSA of high-\(\chi\) PS-\(b\)-PMMA (\(L_0 = 18.5\) NM)
FOCUS 3 – RTO PRODUCTION EFFICIENCY

Technology developments
- Large application fields
- Advanced process solution

Performances

RTO capabilities
- Fab-like equipments
- Large process versatility
RTO PLATFORM STRENGTHS

1. **Fab flexibility & efficiency management**
   - Regular lot shuttle start
   - Steady maturity increase
   - Cycle time focus

2. **MPW platform**
   - Confidentiality
     - Validate private design Ips
   - Fast transfer opportunity
     - Direct learning on production-like platform
• **Shuttle lot concept**
  1. Recurrent lot start on core route technology
  2. Optimize engineering on key process module

• **Advantages**
  1. Regular lot start
     • Mature process flow maturity
     • Progressive data extraction results
     • Easy way to adapt work plan
  2. Reduce cycle time engagement by
     → Raising process maturity on full process flows
     → Pushing in-line controls
  3. Maintain engineering on critical R&D blocks

*Lot speed (step/week) vs normalized maturity (%)*
SILICON PHOTONICS: OPENING OPPORTUNITIES

TOWARDS NEW APPLICATIONS

**Advanced computing**
Neuromorphic, reservoir et quantum

**Optical sensors**
Health, Environment, Automotive

**3D Imaging & LIDAR**
Indoor/outdoor automotive, drone, smartphone etc.

**Computer Interconnections**
MULTI PROJECT WAFER
Silicon Photonics Offer

300mm SOI substrate

- 310 nm Si
- Multilevel silicon patterning
- Selective Ge epitaxy
- Heater
- 2 metal layers

PDKs available

- O & C-band
- Passive & active devices
- Cadence PDK
- Synopsys PDK
- Mentor PDK
- Luceda PDK

Lot shuttles

Multiple runs per year
- April & November

Applications

- Telecom
- Datacom
- Computercom
- LIDAR
- ...

Add-ons

- SiN layer
- III-V on Si
- 3D integration

Technology platform
ECOSYSTEM DEVELOPMENT AROUND PATTERNING FOR PIC DEVICE

AIMS
→ Optimize waveguide performance
→ Develop robust DKM
→ Rise maturity & cycle time

Photonics waveguide

OPC flow output

OPC & MDP

MASK MANUFACTURING

DEVICE MANUFACTURING

FINAL OPTICAL/ELECTRICAL RESULTS

Data Correlation

Device performance results

Mask metro/def

Wafer metro/def

CONFIDENTIAL
• RTO ecosystem
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RTO EFFICIENCY

Technology development
- Large application fields
- Advanced process solution

Performances
- Cycle time commitment
- Constant maturity improvement

RTO capabilities
- Fab-like equipments
- Large process versatility
THE INNOVATION VIRTUOUS LOOP OF RTOs

Device test? Material? Process?

R&D fab

Substrate
CMOS
Power
LED
3D
Display
Photonique

Technology offer
Innovative solution
Shared NRE

Manufacturing
Cycle time
Technology maturity

Fab mission
Performance progress
Ready to transfer

Process flow
Module
Full block

Outcome

Demonstrator
Testchip prototype
ACKNOWLEDGEMENTS

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• French National funding (BPI) : REX-7
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• Special thanks : R Tiron, C Navarro, C Couderc,