Sustainable and “Green” Lithography using Advanced Mask Technologies

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Contents

- Introduction
  ✓ Semiconductor device and lithography roadmap

- Sustainable “Green” Lithography Options
  ✓ Why “Green”?  
  ✓ Optical Lithography Extension  
  ✓ Emerging Lithography

- Conclusions
Introduction ~ Device scaling trends

✓ MPU/ASIC minimum dimension will continuously shrink.

*IRDS 2020 SPIE Meeting
# Lithography options for Lines & Spaces

<table>
<thead>
<tr>
<th>Semiconductor Product node</th>
<th>Production Year</th>
<th>Minimum lithographically defined half pitch for MPU and DRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2018</td>
<td>2020</td>
</tr>
<tr>
<td>&quot;7nm&quot; Logic Node</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18nm DRAM</td>
<td>18</td>
<td>15</td>
</tr>
<tr>
<td>&quot;5nm&quot; Logic Node</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>15</td>
<td>12</td>
</tr>
<tr>
<td>&quot;3nm&quot; Logic Node</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&quot;2.1nm&quot; Logic Node</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14nm and 11nm DRAM</td>
<td>8</td>
<td>8.4</td>
</tr>
<tr>
<td>&quot;1.5nm&quot; Logic Node and below</td>
<td>8</td>
<td>8.4</td>
</tr>
<tr>
<td>&lt;10nm DRAM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **ArF QP Possible**
- **EUV SP Possible**
- **EUV DP Possible**
- **Narrow Options**
- **193nm QP EUV**
- **193nm QP EUV NIL**
- **193nm QP EUV DP NIL DSA**
- **EUV DP High NA EUV DSA plus EUV**

*IRDS 2020 Summer Public Meeting*
# Lithography options for Holes

<table>
<thead>
<tr>
<th>Semiconductor Product Node</th>
<th>Minimum Pitch (nm)</th>
<th>Production Year</th>
<th>2018</th>
<th>2020</th>
<th>2022</th>
<th>2025</th>
<th>2028</th>
<th>2031</th>
<th>2034</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Minimum hole pitch (DRAM, MPU, VCAH)</td>
<td>Estimated cut pitch</td>
<td>51</td>
<td>42</td>
<td>34</td>
<td>30</td>
<td>23</td>
<td>23</td>
<td>22</td>
</tr>
<tr>
<td></td>
<td>Minimum VCAH, Contact and via type pitch</td>
<td>Possible Option</td>
<td>51</td>
<td>42</td>
<td>34</td>
<td>30</td>
<td>23</td>
<td>23</td>
<td>22</td>
</tr>
</tbody>
</table>

### Notes:
- **EUV SP Possible**: EUV Single-Photoresist possible.
- **EUV DP Possible**: EUV Double-Photoresist possible.
- **High NA EUV DP**: High numerical aperture EUV double-photoresist.
- **NIL**: Not Implementable/Not Likely.
- **4 Af-F exposure**: More than 4 ArF exposure.

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Introduction ~ Challenge in EUV mask patterning

- from ArF multi-patterning to EUV single patterning -

Higher mask pattern density will make much longer writing time.


IWAPS 2021
Challenges in EUV mask

- EUV mask needs complex materials and new mask processes.

Mask Blank Structures Comparison

<table>
<thead>
<tr>
<th>Material/Layer</th>
<th>EUV</th>
<th>ArF</th>
</tr>
</thead>
<tbody>
<tr>
<td>absorber layer</td>
<td>TaN</td>
<td>Ar-Cr</td>
</tr>
<tr>
<td>capping layer</td>
<td>Ru</td>
<td>MoSi</td>
</tr>
<tr>
<td>reflective layer</td>
<td>Mo-Si (40 pairs)</td>
<td>Mo-Si (40 pairs)</td>
</tr>
<tr>
<td>substrate</td>
<td>LTEM</td>
<td>LTEM</td>
</tr>
<tr>
<td>back side film</td>
<td>CrN</td>
<td>Qz</td>
</tr>
</tbody>
</table>

- >80 layers, 6 materials
- 3 layers, 3 materials
DNP established the EUV process with hard mask technology and low sensitivity PCAR resist, and MBMW.

“5nm node” EUV mask requires 60nm minimum main feature on mask.

Our EUV mask process can achieve under 30nm resolution for L/S pattern, and under 40nm for Hole patterns, which satisfied “5nm node” requirements and even for “3nm node” target of 48nm main feature.
Mature nodes $\geq 130\text{nm}$ are still major part of devices.
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Why “Green”?  

“Green Growth Strategy Through Achieving Carbon Neutrality in 2050”  *

[1] Promotion of energy demand efficiency and CO2 reduction through digitization  
(Green by Digital)  

[2] Energy conservation and greening of the digital equipment and information and telecommunications industries themselves  
(Green of Digital)  

✓ For “Green Digital Society”, our semiconductor industry has an important role in carbon neutralization.
Advanced node device manufacturing using advanced lithography need more energy.

Manufacturing energy per wafer by nodes. From iN28 to iN3

Electrical energy used per wafer for different lithography options.

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Curvilinear ILT Started a Decade Ago

Fast Inverse Lithography Technology

Daniel S. Abrams, Linyong Pang
Luminescent Technologies, Inc., 650 Castro Street, Suite 220, Mountain View, CA 94041, U.S.A.

* “Inverse lithography technology: 30 years from concept to practical, full-chip reality”, Leo Pang, JM3 2021

IWAPS 2021
Process window expanded by ILT

Curvilinear ILT Produces the Best Process Window

The base study on conventional fracturing is courtesy of Byung-Gook Kim, et al., PMJ 2009

*“Inverse lithography technology: 30 years from concept to practical, full-chip reality”, Leo Pang, JM3 2021

✓ Aggressive ILT expanded lithography process window, e.g. depth of focus, drastically.
Process window expanded by ILT

✓ ILT by TrueMask™ showed much wider lithography process window for random contacts.

* "Inverse lithography technology: 30 years from concept to practical, full-chip reality", Leo Pang, JM3 2021

IWAPS 2021
ILT issues in mask making

* Aggressive ILT patterns need huge number of shots in conventional VSB mask writer.

IWAPS 2021
MBMW principle - difference between VSB and MBMW -

VSB = Vector Scan Beam

- Variable Shaped Beam mask writer
- One shaped vector beam
- Writing time dependency
  #shot counts
  #resist sensitivity

MBMW = Multi Beam Mask Writer

- Multi Fixed Beam Mask Writer
- 262-thousand raster beams
- Writing time independency for pattern complexity
- Designed for mid and low sensitivity resist

✓ MBMW is essential for complex mask patterning.
High-End mask need over 700 Gshots/pass for VSB.

MBMW using raster scan system, so no impact from shot counts, only depends on writing area.

Massive parallel beams enable to use lower sensitivity resists, which make improvements in resolution and fidelity without writing time penalty.

✓ MBMW technology shows good productivity.
MBMW is the solution for high density mask patterning

- from ArF multi-patterning to EUV single patterning -

MBMW can write a mask with constant writing time not depend on pattern density.


**IWAPS 2021**
Pattern Position Accuracy of MBMW

- Performance of MBMW with low sensitivity PCAR EUV process.

140mmx140mm cross pattern

3 sigma: 0.9/0.81 (X/Y)
Test mask reg map
(tool check pattern)

100mmx135mm Device mask

3 sigma: 1.35/1.21 (X/Y)
Production mask reg map

✓ MBMW EUV process can achieve pattern position accuracy for 5nm.

Target spec:<1.5nm

MBMW EUV process can achieve pattern position accuracy for 5nm.

IWAPS 2021
Global CD Uniformity of MBMW

- CDU performance of MBMW with low sensitivity PCAR EUV process.

Target spec:<1.5 nm

✓ Global CDU can achieve <1.0nm for both main and assist feature.
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Emerging Lithography ~ Nanoimprint

Process flow of NIL

Advantages of NIL

- Single exposure, simple process, low CoO
- Low power consumption
- High resolution, no optical limit
- 3-D pattern transfer capability

* “Nanoimprint Template Development by New Fabrication Method and Its Application”, Kouji Ichimura, et al., SPIE Advanced Lithography 2021
Emerging Lithography ~ Nanoimprint

Examples of 3-D nano-imprint templates

- Dual damascene template
- Multi-step template
- High aspect ratio small pillar
- Slope templates

* “Nanoimprint Template Development by New Fabrication Method and Its Application”, Kouji Ichimura, et al., SPIE Advanced Lithography 2021
Based on our simulation, NIL is more than 10 times energy effective and “Green”, compared with other advanced lithographies.

* Simulated by DNP, single layer adoption, 15nm L/S
Conclusion

1. Semiconductor device roadmap shows continuous scaling at most advanced nodes with EUV lithography, and in parallel we need huge volume of mature node devices to sustain the expanding digital society with high energy efficiency and appropriate cost.

2. Inverse Lithography using the curvilinear features is the attractive technology to extend the DUV lithography with improved process window, but with mask making challenges caused by very complex patterns.

3. MBMW, the multi-beam mask writer, has been successfully filled the gap with excellent productivity and accuracy using massive parallel e-beams and the air bearing stage.

4. Nanoimprint lithography has the potential to enable scaling with simple, energy and cost-effective manners.

5. DNP is providing various mask solutions using advanced technologies, such as MBMW, and will support wide range of lithography options in future.
Thank you for your attention.

謝謝！