leti
cea tech

THE VIRTUOUS CIRCLES OF THE RTOS

HOW TO SUPPORT AND BOOST TECHNOLOGY DEVELOPMENTS FROM MATERIALS TO INTEGRATION

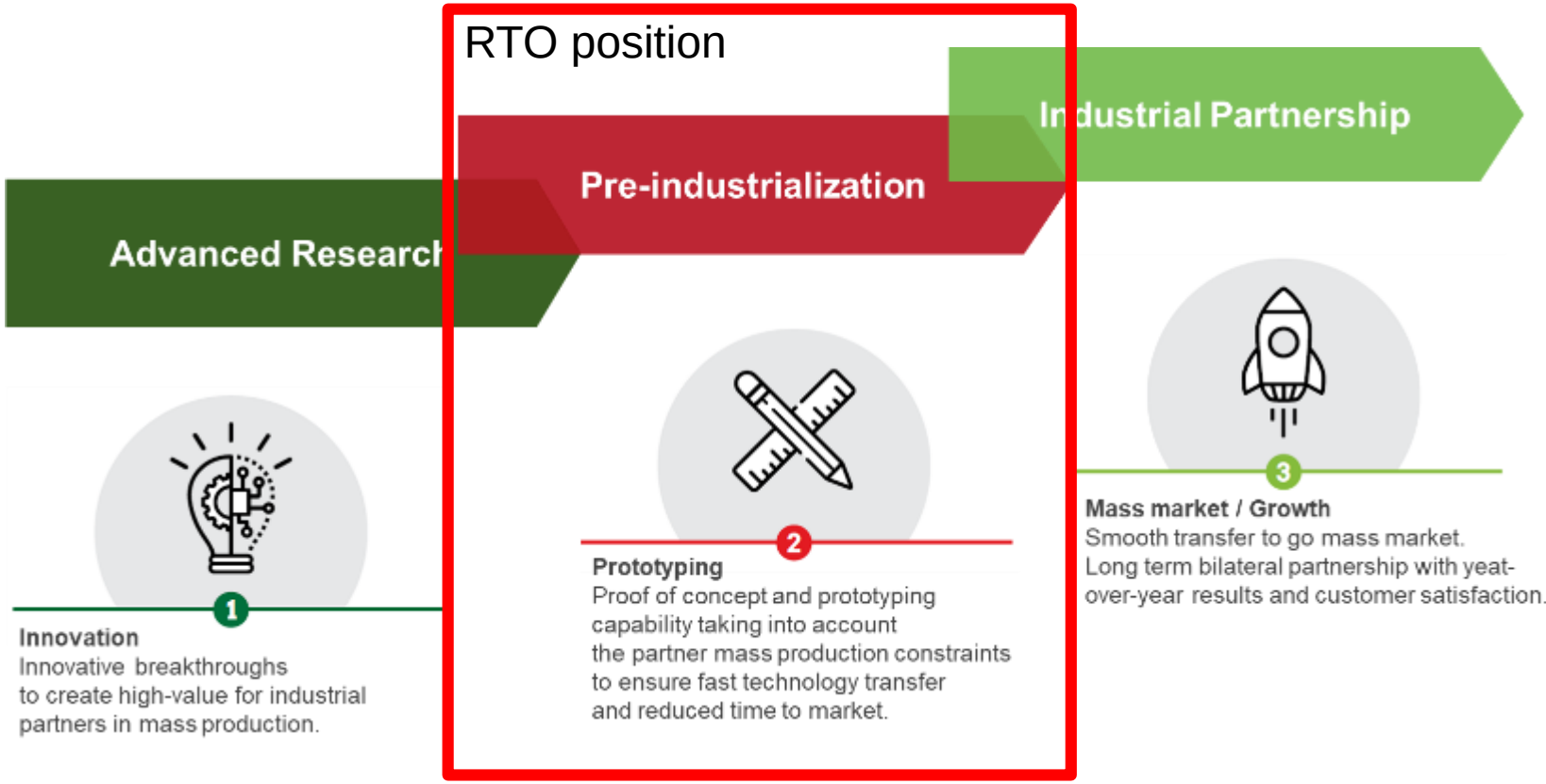
LAURENT PAIN, CATHERINE EUVRARD-COLNAT, GUIDO RADEMAKER

OUTLINE

- **RTO ecosystem**
- **3 focuses on RTO efficiency parameters**
  - Fab capabilities
  - Technology development
    - CMP program
    - DSA patterning
  - Fab performances
- **Conclusions**

WHAT IS A RTO?

- **Definition**
  - RTOs are non-profit organizations with public missions to support society providing
    - Research and development, technology and innovation services to enterprises, governments and other clients…" (EURAB 2005).
    - Their mission is to help companies move "one step beyond" their existing capabilities
    - Reduce the risks associated with innovation for a faster rate of economic development



CEA-LETI RTO KEY FIGURES

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“3rd Innovative Public Research Organization Worldwide” 2012 -2020

Derwent™
A Clarivate Analytics company

- Since **1967**
- **2,000** people

Patents:
- > 3,000 in portfolio
- 40**%** under license agreement

Startups:
- 68 created for 20 years (75% in activity)

Cleanrooms:
- 500 state-of-the-art equipment in 200 et 300 m²
- 10 000 square meters cleanroom

Budget:
- 315 M€
- 85% from R&D contracts

UNIQUE ECOSYSTEM: 3 VALLEYS

Microelectronics Valley

6,000 direct jobs

Display Valley

500 jobs expected in 2024

Imager Valley

1,500 direct jobs

OUTLINE

- RTO ecosystem
- **3 aspects of RTO efficiency parameters**
  - Fab capabilities
  - Technology developments
    - CMP program
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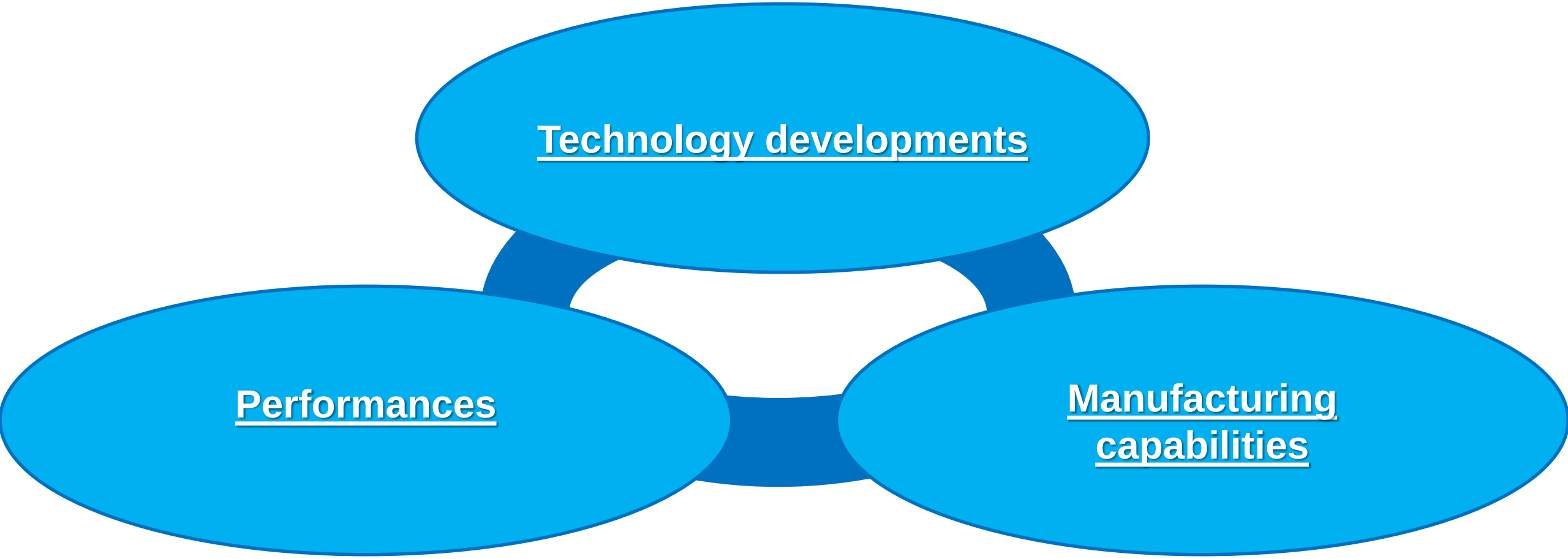
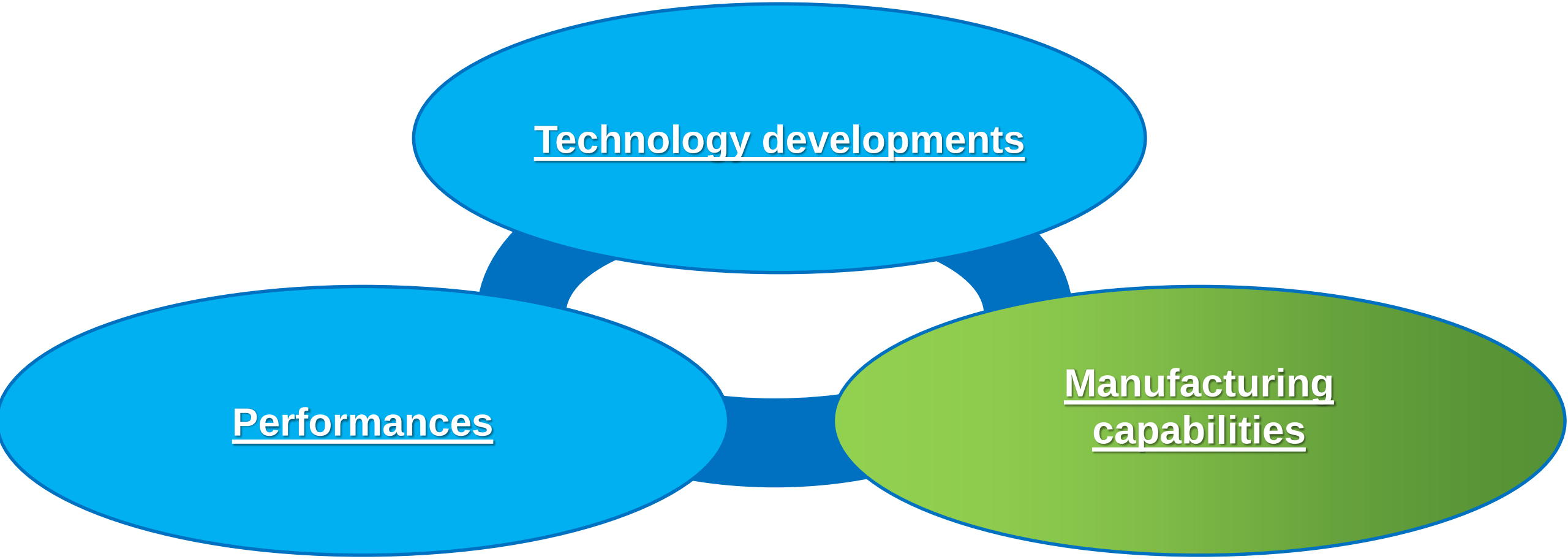
  - Fab performances
- Conclusions

3 FACES OF RTO EFFICIENCY

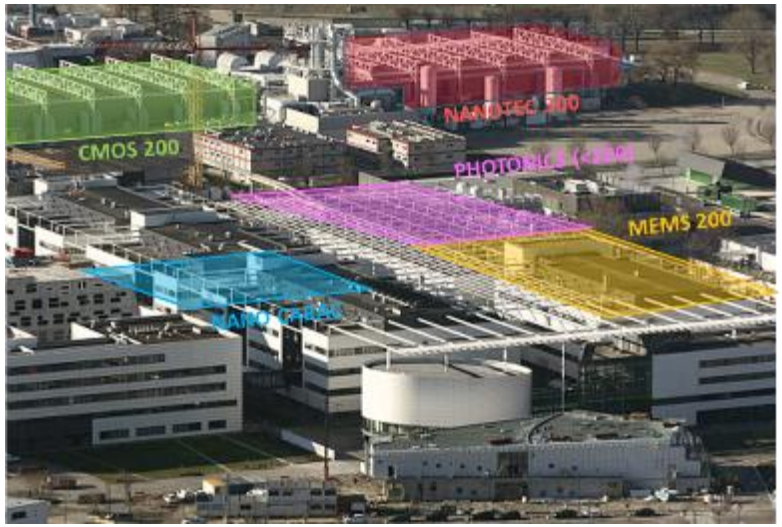


FOCUS 1 – Manufacturing capability



LETI TECHNOLOGY PLATFORM CAPABILITIES

- **300mm & 200mm Si components Platforms**
  - **~270**@200mm equipments
  - **~105**@300mm equipments
  - 5600 square meters Cleanroom - ISO3-5
  - 24/7 operations
- **200mm MEMS Platform**
  - **~130**@200 mm equipments
  - 2200 square meters - ISO 4-5
  - 24/7 operations
- **Substrates <200 mm, III-V and II-VI Platform**
  - **~230** @ various diameter equipments
  - 1000+1000 square meters - ISO 4-5
  - 1shift/day
- **Nano-CHARACTERIZATION Platform**
  - **~ 40** huge equipments
  - 2200 square meters
  - 8 centers of competences



Concentration of Means to Address Large Photonics Challenges Closely with the Silicon Platform

MATURE & UP-TO-DATE PLATFORMS

FC300
DtW
High Speed

Direct
hybrid
bonding

193i
Scanner

Laser
Annealing

Dielectric
Contact
Etching

Low Temp
Epi
MOCVD

PCM
Endura

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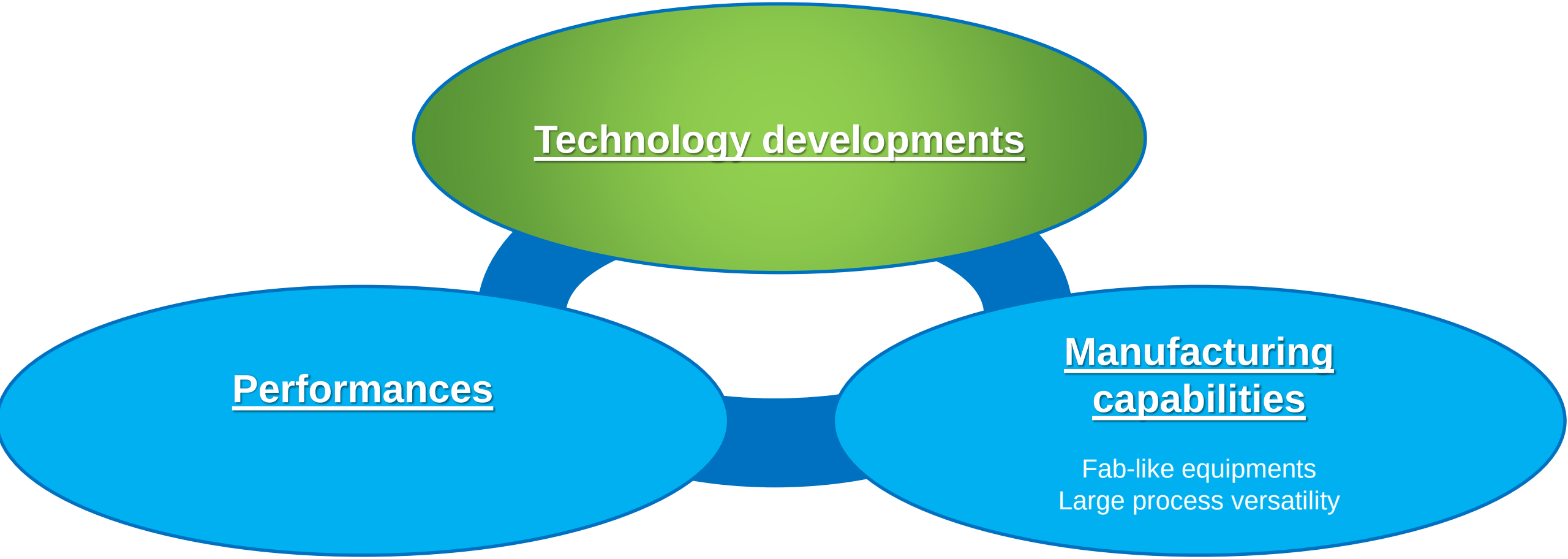
FOCUS 2 – Technology innovation

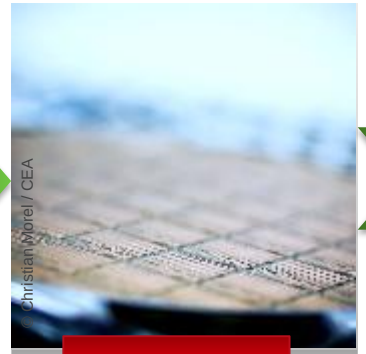


TECHNOLOGY DEVELOPMENT FUELS INNOVATION

ARCHITECTURES

RF, Neural Network, Smart Sensors, Actuators, LiFi …

MATERIALS



SOI, SiC GAN, III-V, GST, polymer, slurry …

PROCESS INTEGRATION

Module and process flow Patterning – deposition - surfacing

PACKAGING

Pixel Array, Memories LNA, PA, PMUT, Photo-Acoustic…

COMPONENTS & DEVICES

LED, T-MOS RF Switch, MEMS, NVM-RAM, TSV …

MASTERING THE DEVELOPMENT OF INDUSTRIAL TECHNOLOGY SOLUTIONS

From materials to device

CLOSE PARTNERSHIPS WITH KEY SUPPLIERS

CMP WORK PROGRAM EXAMPLE

Deposition

- Applied Materials
- Solmates
- aveni

Patterning

- Lam Research
- ASML
- EVG
- SCREEN
- aselta
- TEL
- Mentor, A Siemens Business
- JSR Corporation

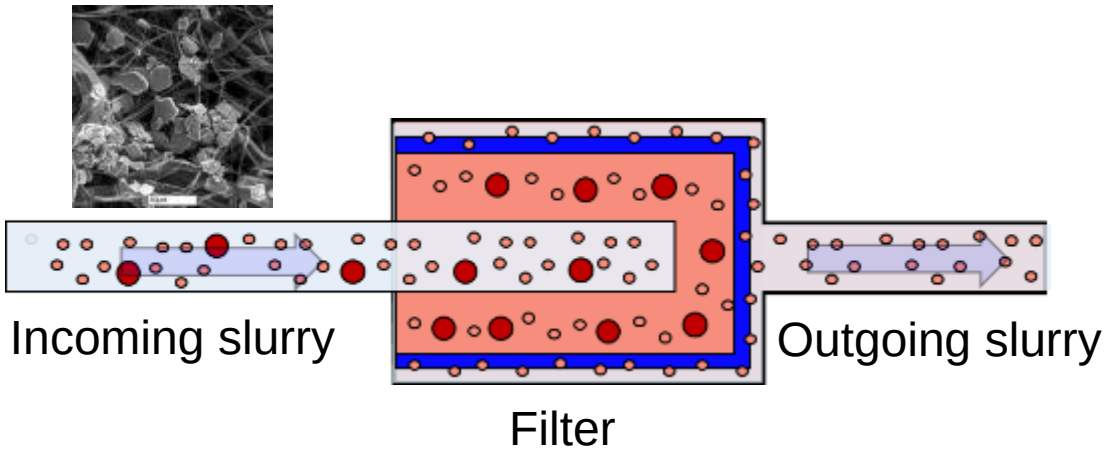
Surfacing

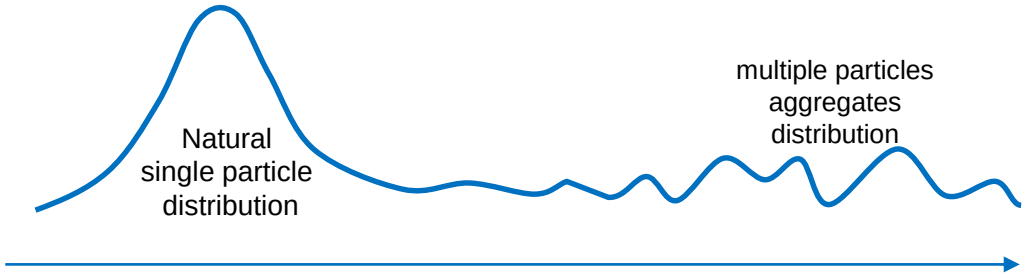
- EBARA
- Applied Materials
- Entegris
- EVG
- soitec
- Nagase ChemteX, Nagase Group
- SCREEN

Metro/Charac

- unity SC
- KLA
- Applied Materials
- Rigaku
- Entegris
- BRUKER

CMP CHALLENGE
INCREASE SLURRY LIFETIME W/O YIELD IMPACT ON DEVICE





~10 nm	50 ~ 100 nm	100 ~350 nm	LPC Monitor > 560 nm
New generation slurries for 10 nm node or less	Colloidal SiO2 based particles slurries	Ceria based slurries	Particle agglomerates, gels, particles generated inside the distribution system and inside the polisher

Study & understand filtration efficiency

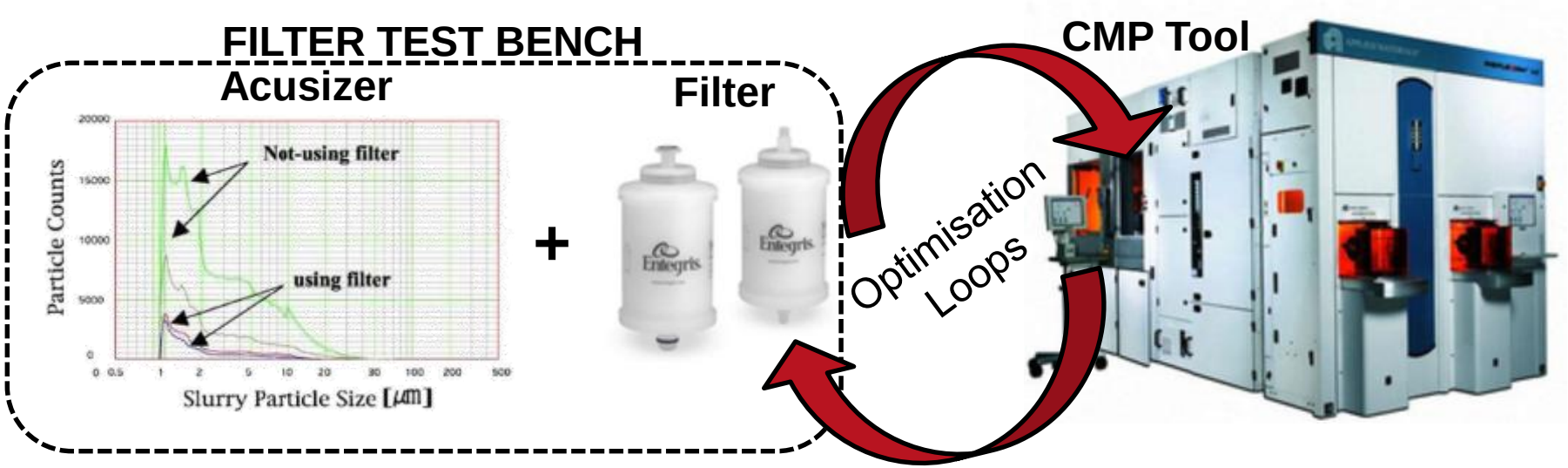
- big particles filtration to prevent scratches defects
- Maintain slurry optimal properties by optimizing natural particle size distribution
  - Removal rate
  - Planarization efficiency
  - Selectivity

OPTIMIZE CMP PROCESS FLOW & EFFICIENCY

1 Filter selection optimization on test Bench
Selection of key monitoring parameters for slurry/filter couples

2 Test best filters set up on CMP tool
Verify CMP process performances on blanket and patterned lot wafers

3 Filter life time optimization
Quantify efficiency gain and perform optimization loops



3 YEARS PROGRAM
CMP PROCESS flow CHAIN OPTIMIZATION

CLOSE PARTNERSHIPS WITH KEY SUPPLIERS

Deposition

- APPLIED MATERIALS
- Solmates
- aveni

Patterning

- Lam RESEARCH
- ASML
- EVG
- SCREEN
- aselta
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Surfacing

- EBARA
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Metro/Charac

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- KLA
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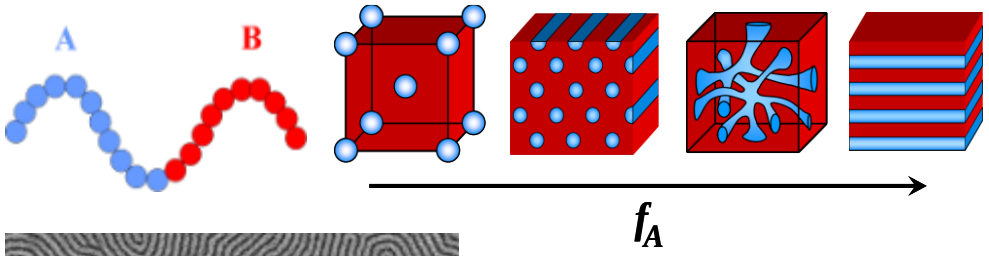
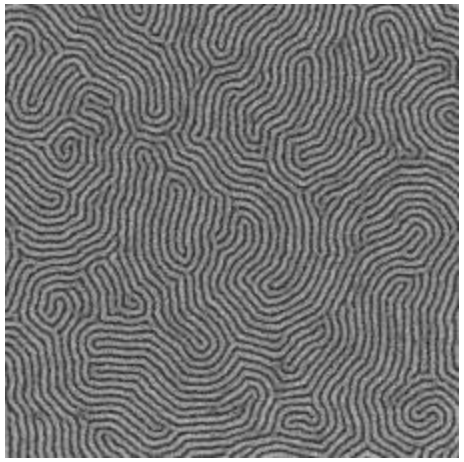
- BRUKER

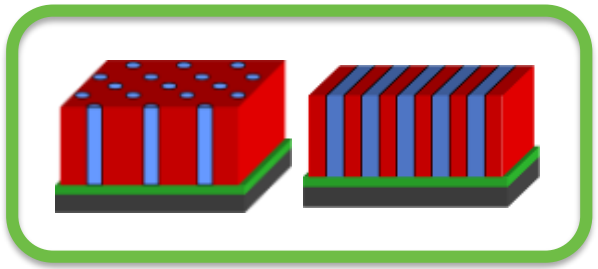
DIRECTED SELF ASSEMBLY CONCEPT

BCP



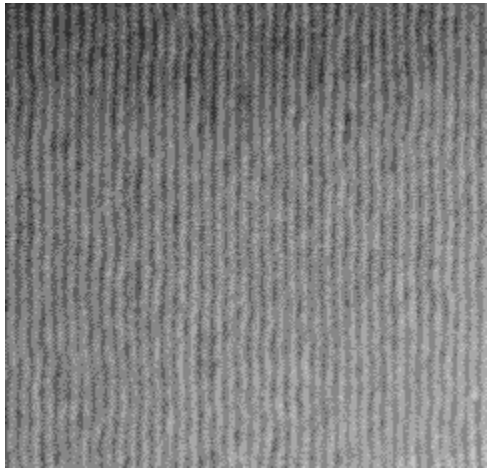


High chi – L0=18nm

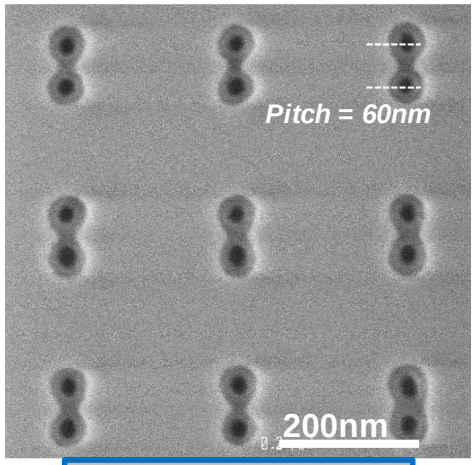


GUIDE

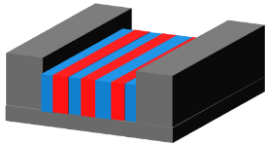
Chemoepitaxy

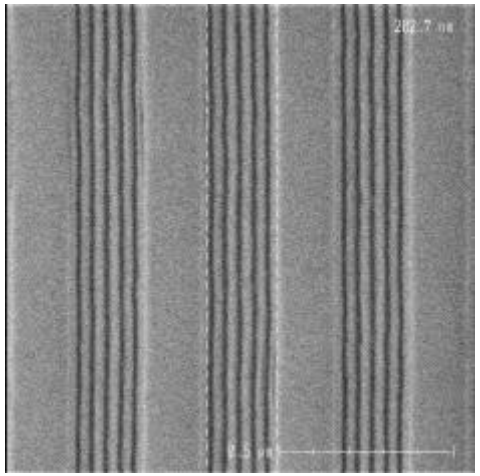


DSA chemoepitaxy with 22nm period PS-b-PMMA
IMB-CNM & Leti collaboration
L. Evangelio et al., talk at 2nd DSA Symposium, Grenoble (France), October 2016



Graphoepitaxy





DSA gaphoepitaxy with 38nm period PS-b-PMMA
G. Claveau et al., J. Micro/Nanolith. MEMS MOEMS 15(3), 031604 (2016)

DSA DEVELOPMENT ECOSYSTEM @LETI

Partnership framework

Industrial

ARKEMA

IDEAL

brewer science

SCREEN TEL

Mentor A Siemens Business LTM

APPLIED MATERIALS NOVA PROCESS INSIGHT

Institutional

Horizon 2020

COLISA – Ion4SET

ECSEL Joint Undertaking

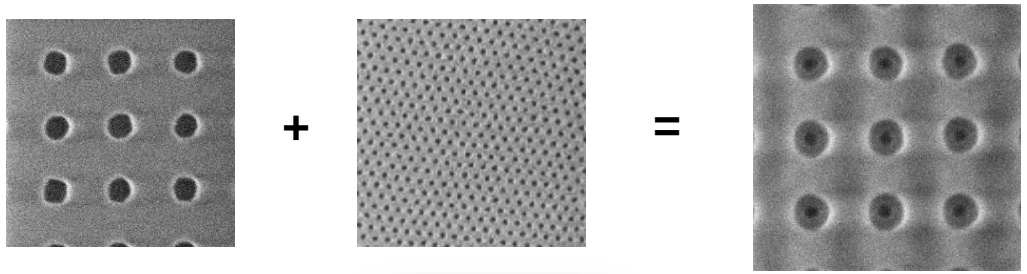
PLACYD – MADEin4

bpifrance

REX-7

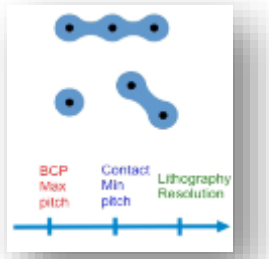
Grapho-epitaxy demonstration
N10 demonstration capability
2012-2018

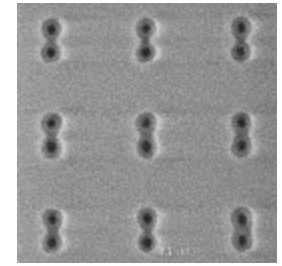
Contact hole shrink and doubling



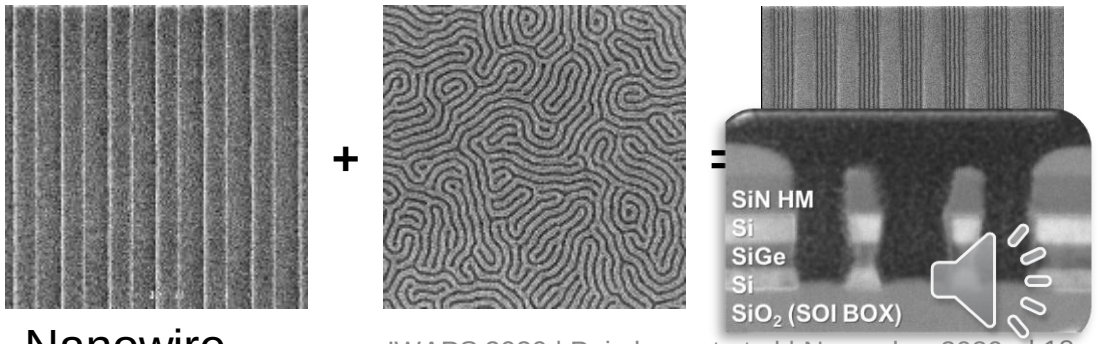
+ advanced OPC

N10



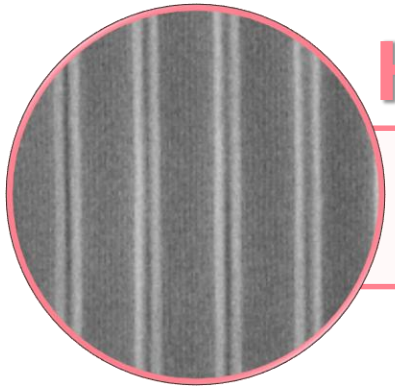


Line/Space patterning



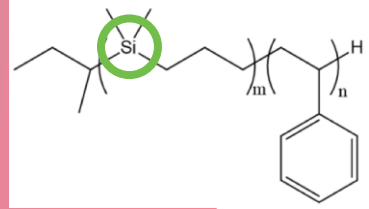
Nanowire

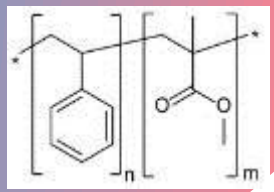
DSA MATERIAL PORTFOLIO



Highχ (L_0<20nm)

- **Mandatory for sub N5 L&S**





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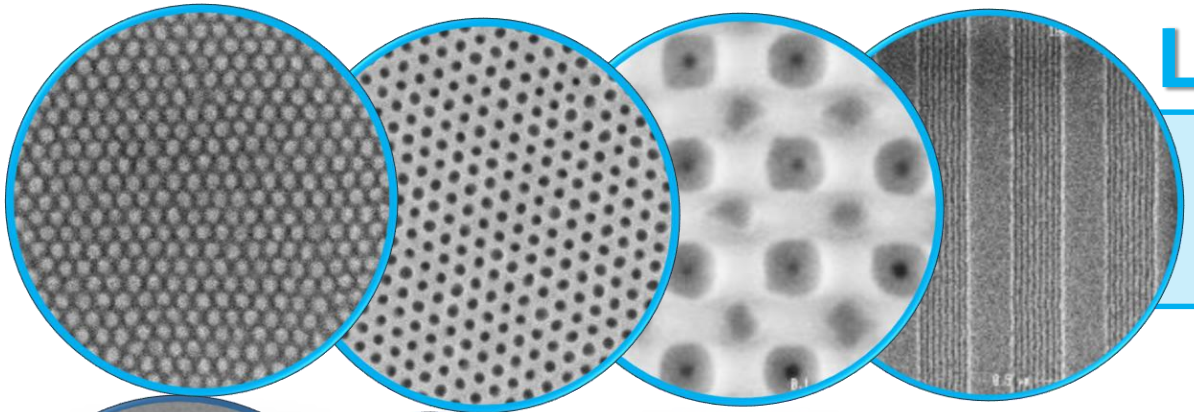
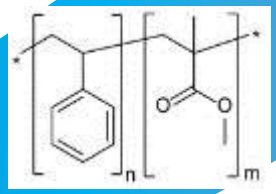
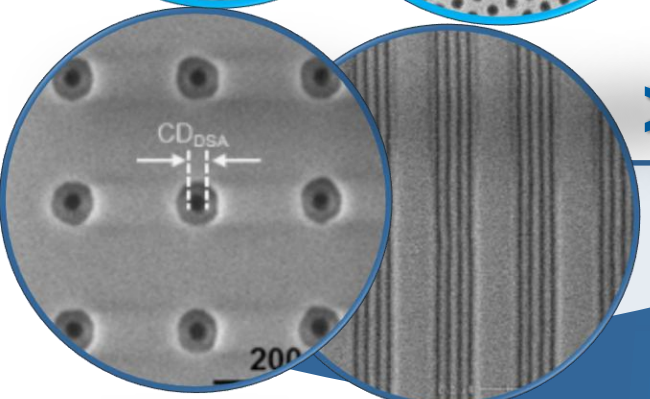


L22 (PS-b-PMMA)

- **Contact : Suitable down to N5**
- L&S : scalable down to N7
- Other application : sensors surface



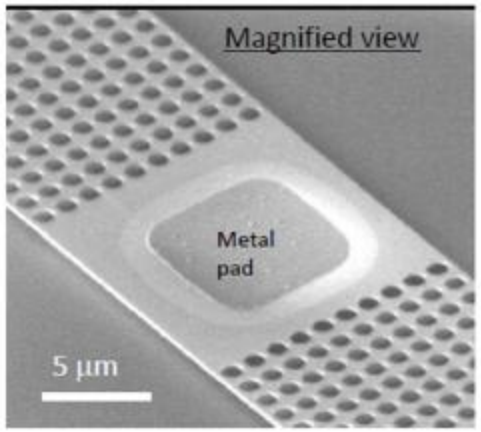


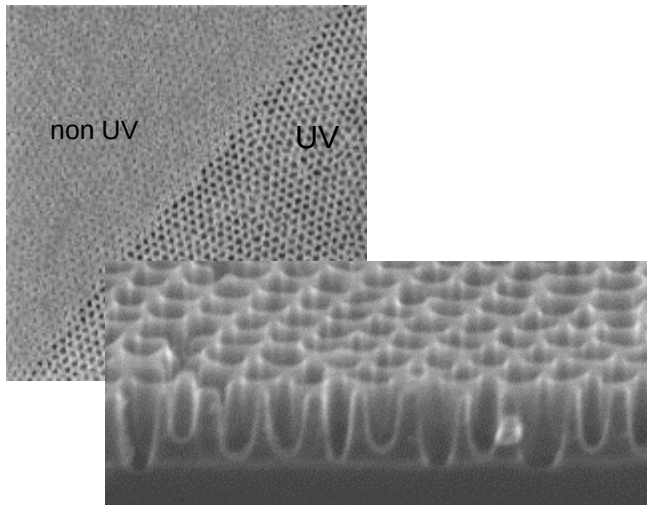
>L38 (PS-b-PMMA)

- **1st Gen DSA materials**
- Main application : contact/via
- Other application : sensors - surface

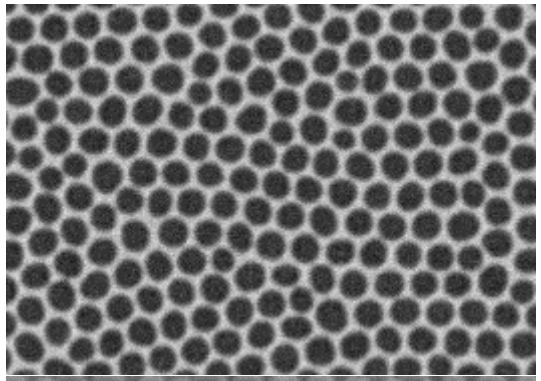
BLOCK COPOLYMERS FOR NON-CMOS APPLICATION

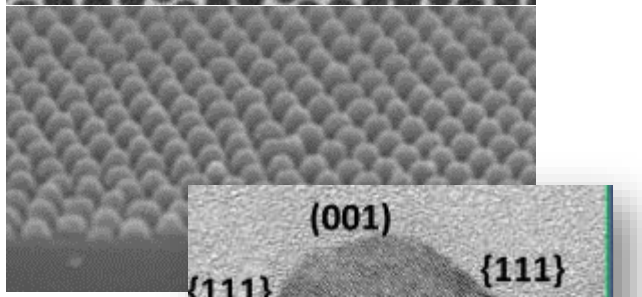
Low-cost surface structuration for MEMS sensor

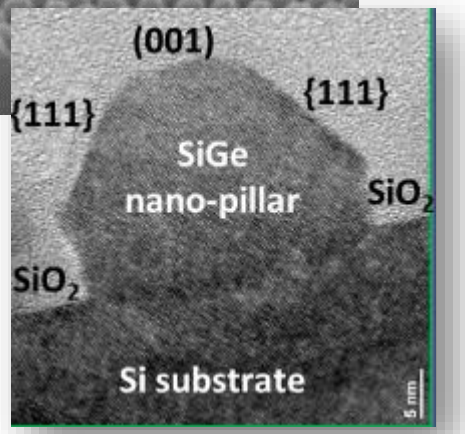




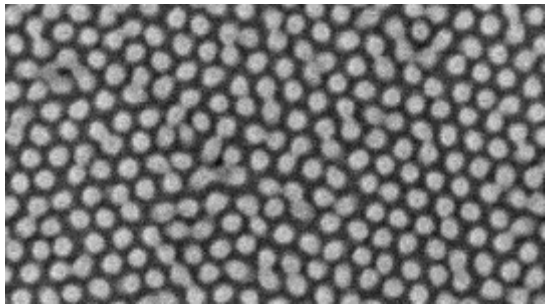
SiGe Epi growth template

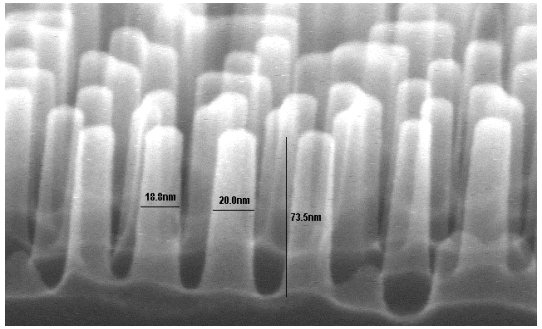


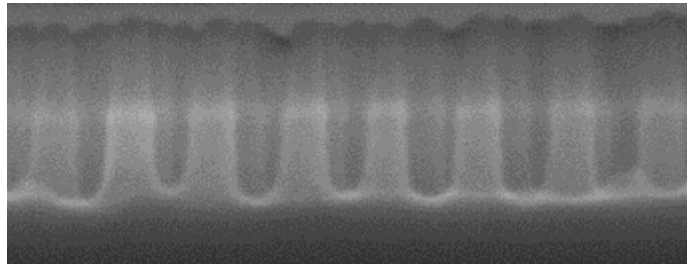




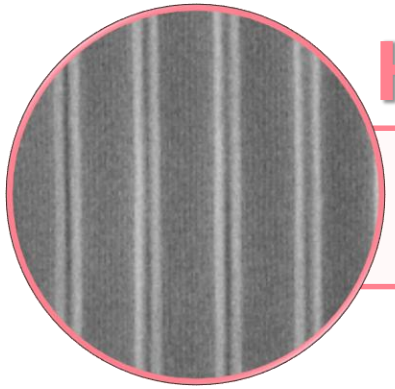
Si nanopillars
Inverted PS-*b*-PMMA matrix
h = 70 nm, Ø 15 nm





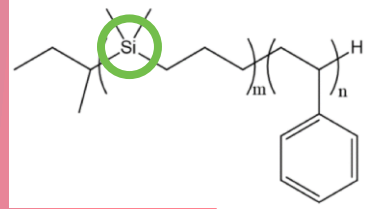


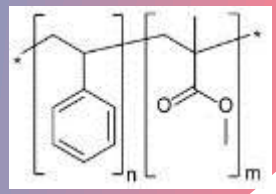
DSA FOR CMOS APPLICATIONS



Highχ (L_0<20nm)

- **Mandatory for sub N5 L&S**





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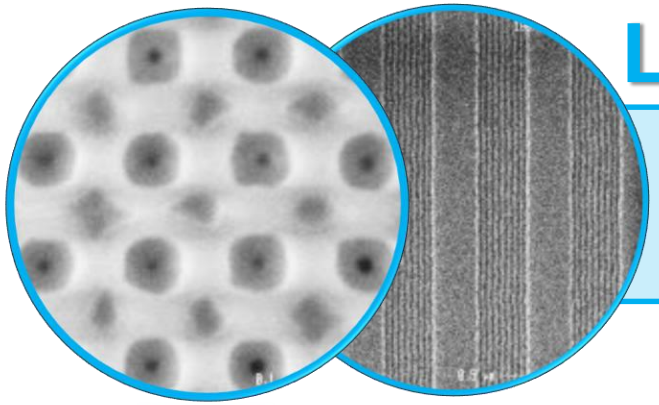

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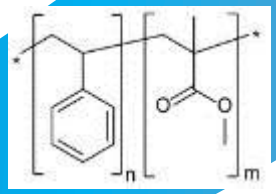

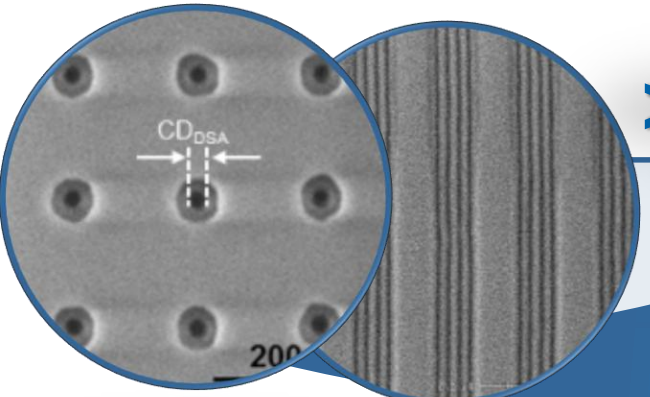

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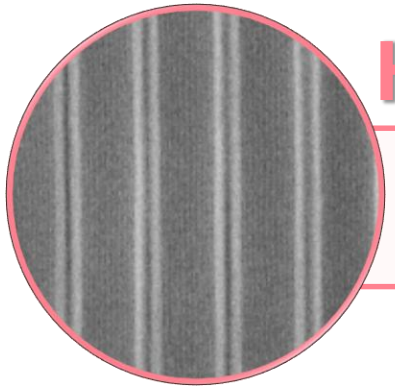
Process Development

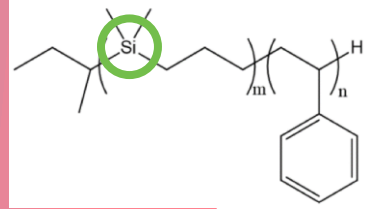
Process ecosystem

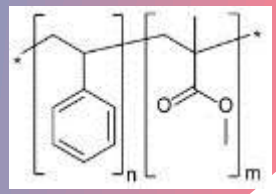
DSA DEVELOPMENTS



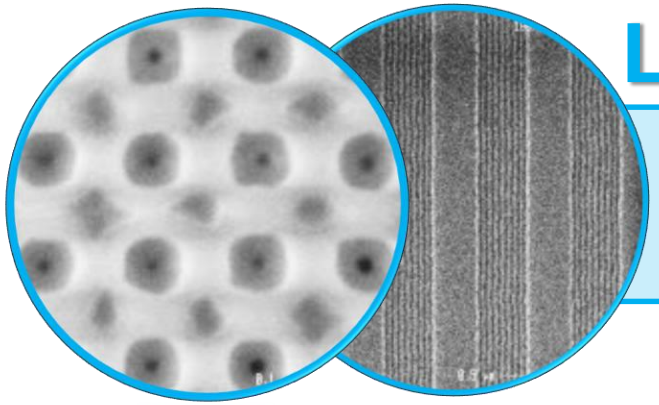
Highχ (L_0<20nm)

- **Mandatory for sub N5 L&S**



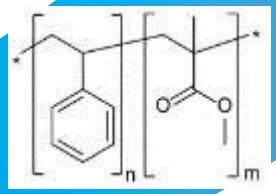


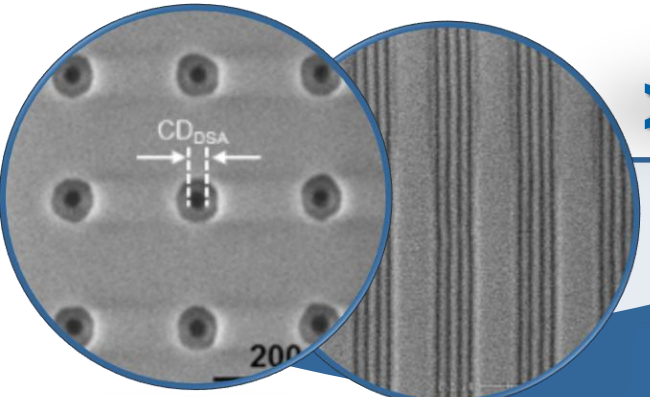
modified



L22 (PS-b-PMMA)

- **Contact : Suitable down to N5**
- L&S : scalable down to N7
- Other application : sensors surface





>L38 (PS-b-PMMA)

- **1st Gen DSA materials**
- Main application : contact/via
- Other application : sensors - surface

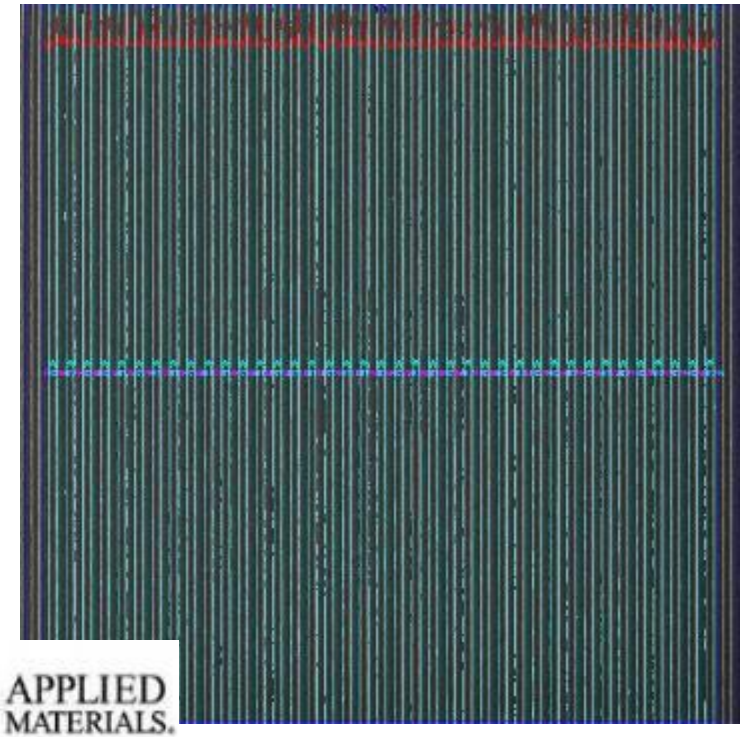
Process Development

Process ecosystem

ADVANCED METROLOGY

Advanced CD-SEM

Low energy (300 V), low # frames
to prevent resist shrink
Large grab for local statistics
Tilted beam metrology

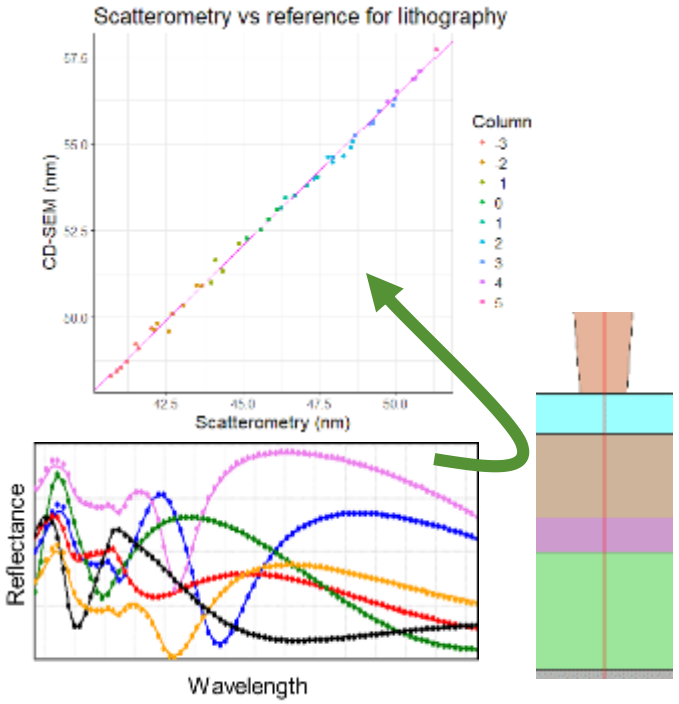


APPLIED MATERIALS

Scatterometry

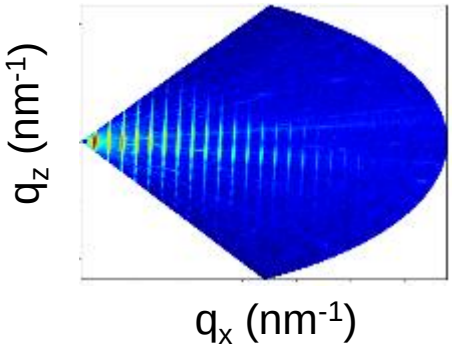
3D metrology at every
process step

TMU = **0.36 nm** (48 pt.)



CD-SAXS/GISAXS

→ Reference for 3D metrology
→ LWR : Extraction of PSD



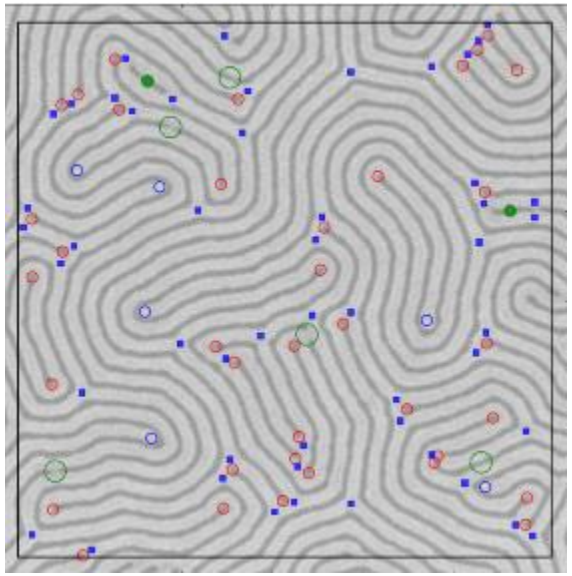
See presentation Freychet et al.
SPIE AL 2020 (parallel session)

Critical-dimension grazing-incidence small angle X-Ray scattering: applications and development

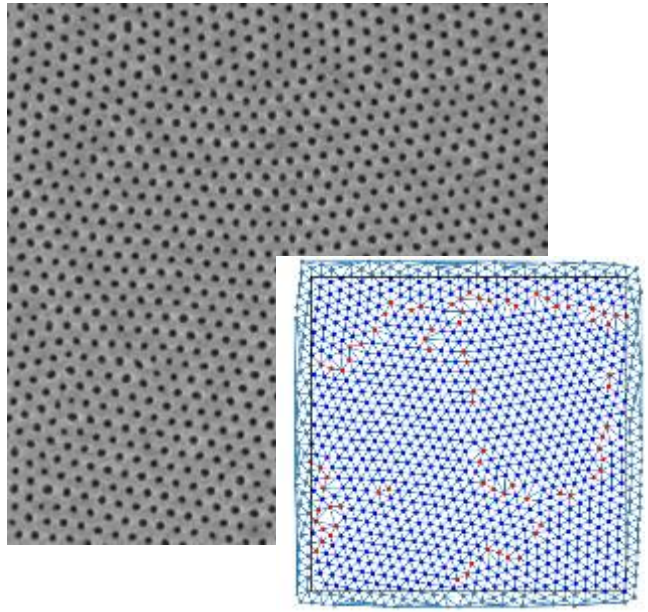
SOFTWARE SUITS FOR MATERIALS & PROCESS EVALUATION

Free surface defect analysis

Line end assembly
for lamellar BCP

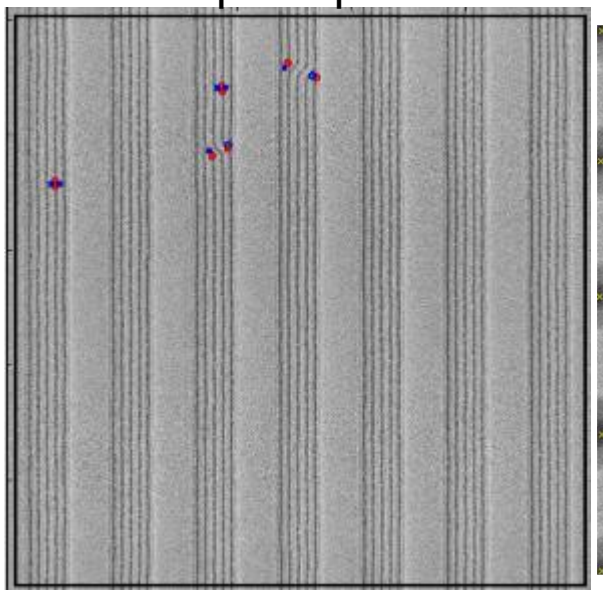


Grain boundaries
for cylindrical BCP

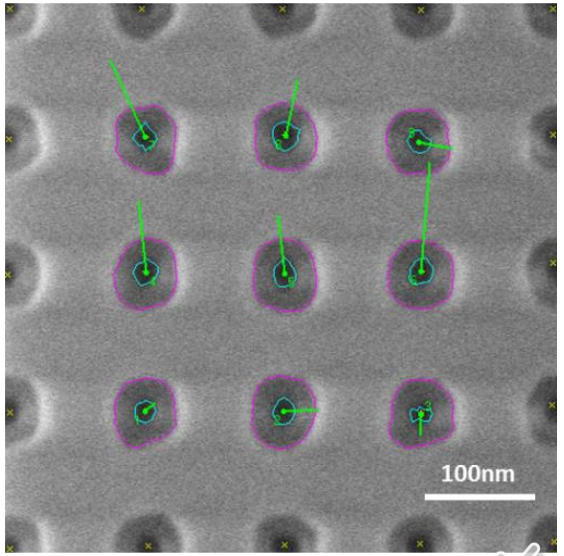


Directed Self-Assembly

Def
Line/space patterns

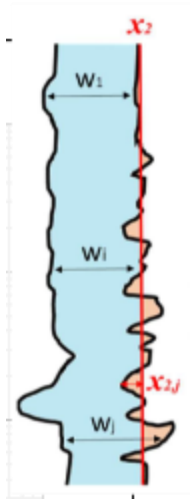


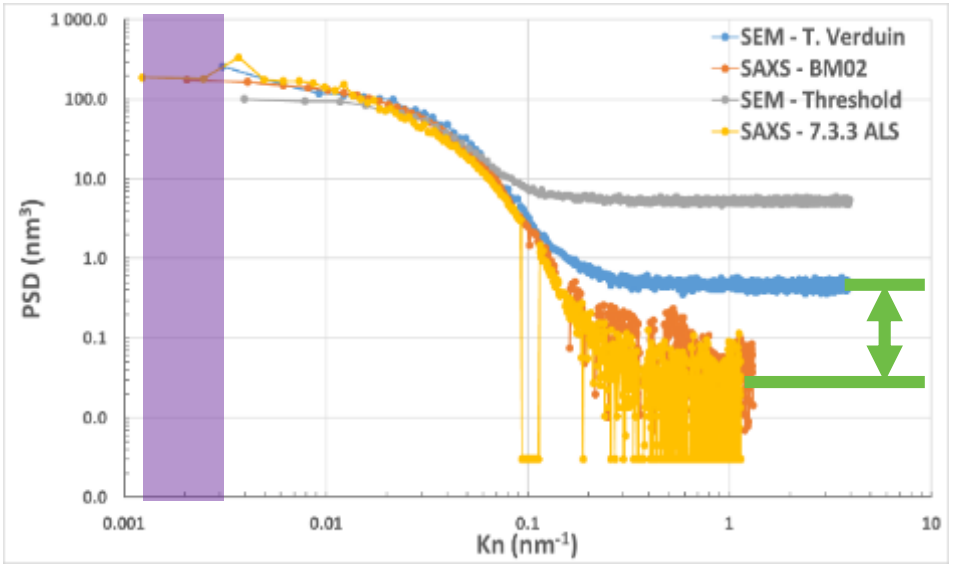
CD, Hole open yield &
Pattern placement error



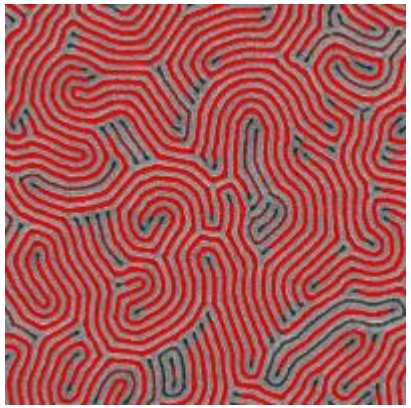
LWR EXTRACTION
POWER SPECTRAL DENSITY (PSD)

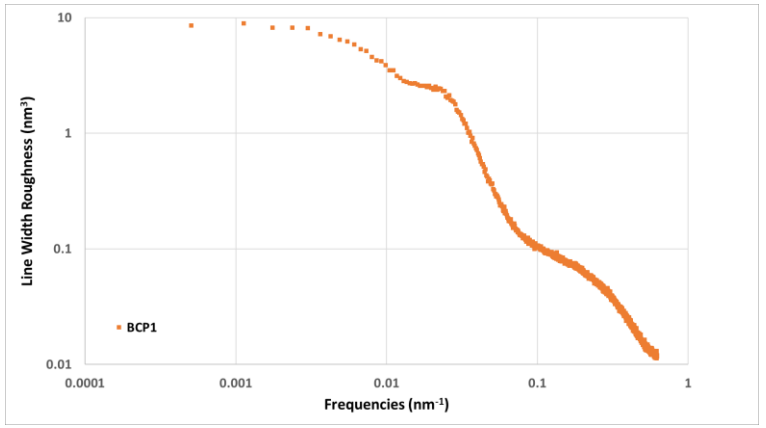
- ***Unbiased* roughness metrology is necessary**
  - Frequential breakdown to correct for CD-SEM noise floor bias
- **Unique reference measurement method by synchrotron radiation (CD-SAXS)**
  - **Measure of lower frequencies**
  - **Lower noise floor at high frequencies**
- **Line width roughness on fingerprint samples for BCP material evaluation**
  - Algorithm development shared with photonic circuit applications





J. Reche, *Dimensional Control of Line Gratings by Small Angle X-Ray Scattering*, Proc. ASMC (2020)



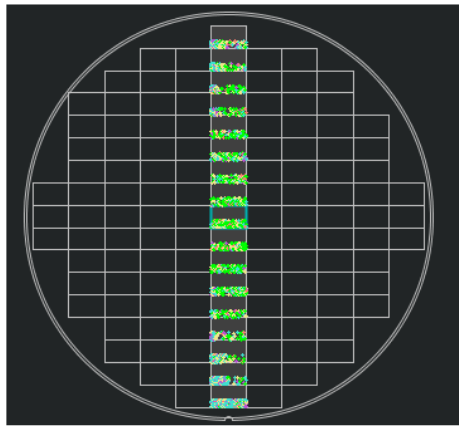


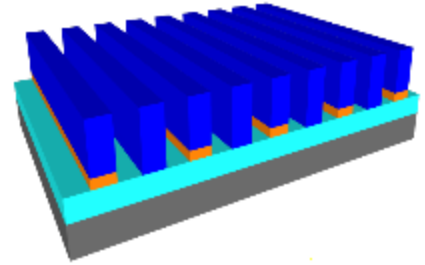
A. Le Pennec, *Block copolymer line roughness measurements via PSD*, Proc. SPIE, 113261I (2020)

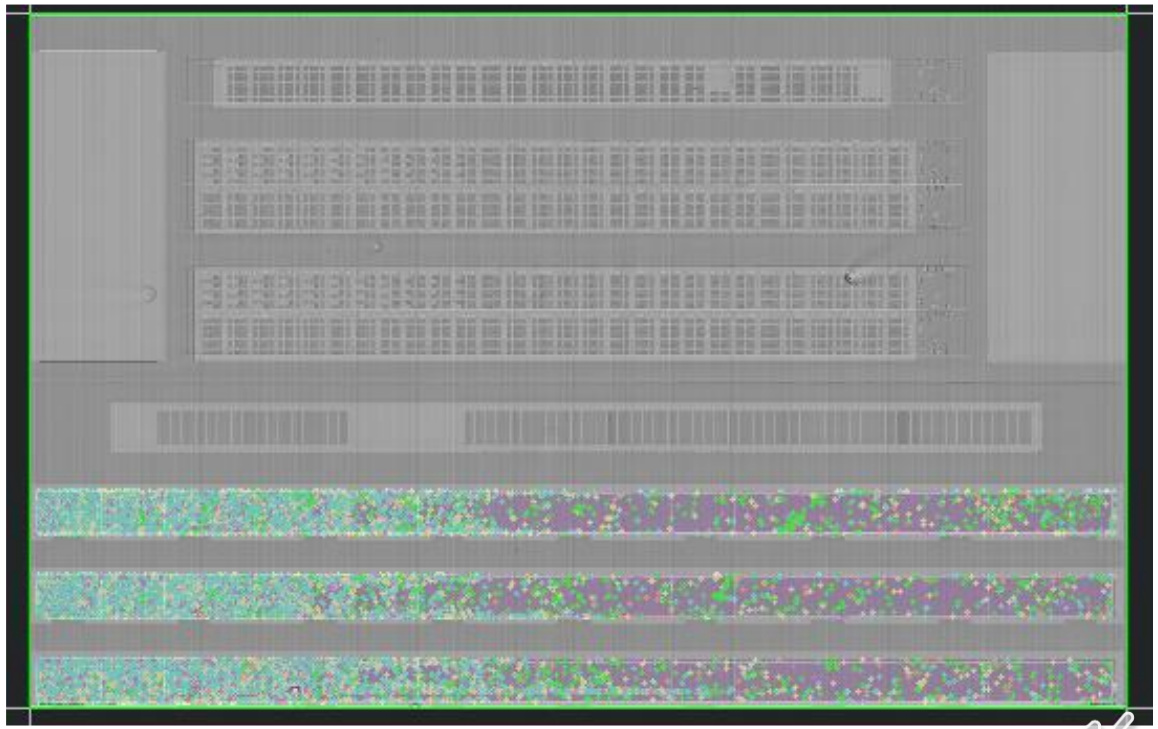
FIRST DEFECT INSPECTION WORK L&S

- **Defect inspection & review:**
  - Applied Materials UVision 8
  - Applied Materials SEMVision G7E

- **Determination of pixel size, polarization and laser power adapted to PS lines (PMMA removed)**



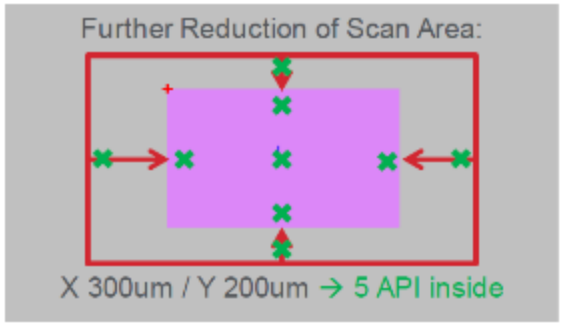


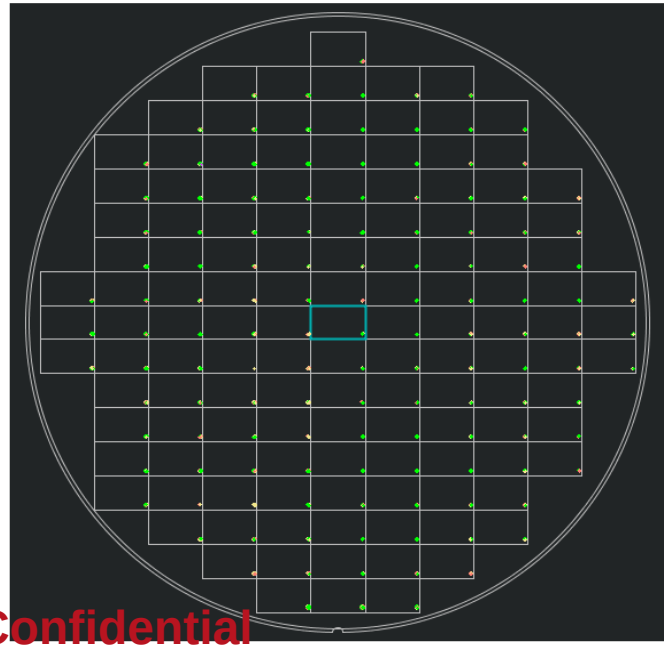


Litho pitch variation = 112 nm – 128 nm

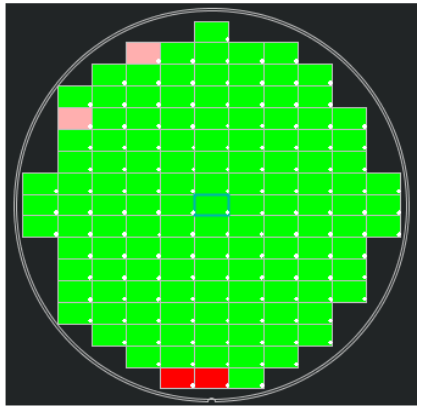
SMALLER DEFECTS EXTRACTION CPAPABILITY

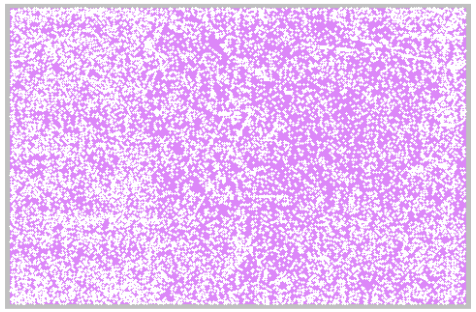
- Reduction of scan area to one shrunk array box
- Adaptation of pixel size and polarization mode



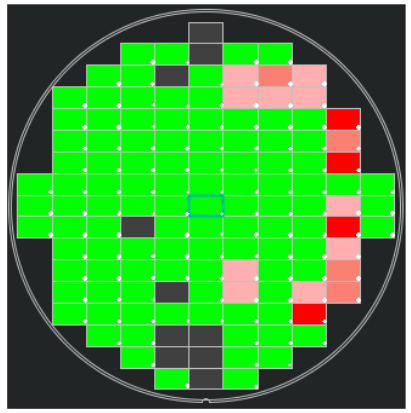


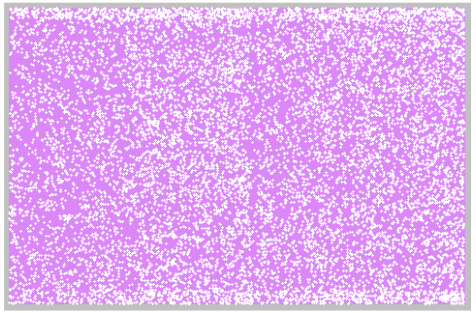
T19S893-P06 Slot 06
Defect Count : 18580



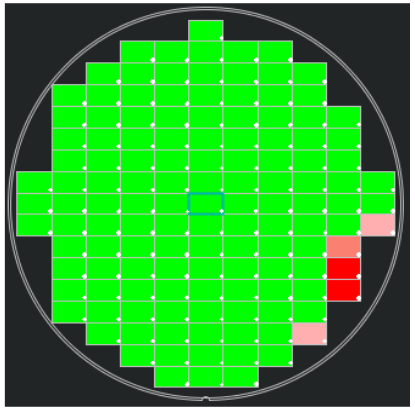


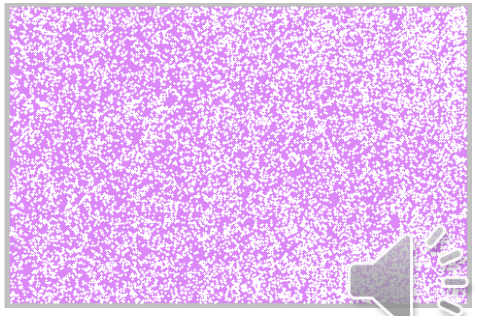
T19S893-P17 Slot 16
Defect Count : 11512





T19S893-P07 Slot 25
Defect Count : 16927





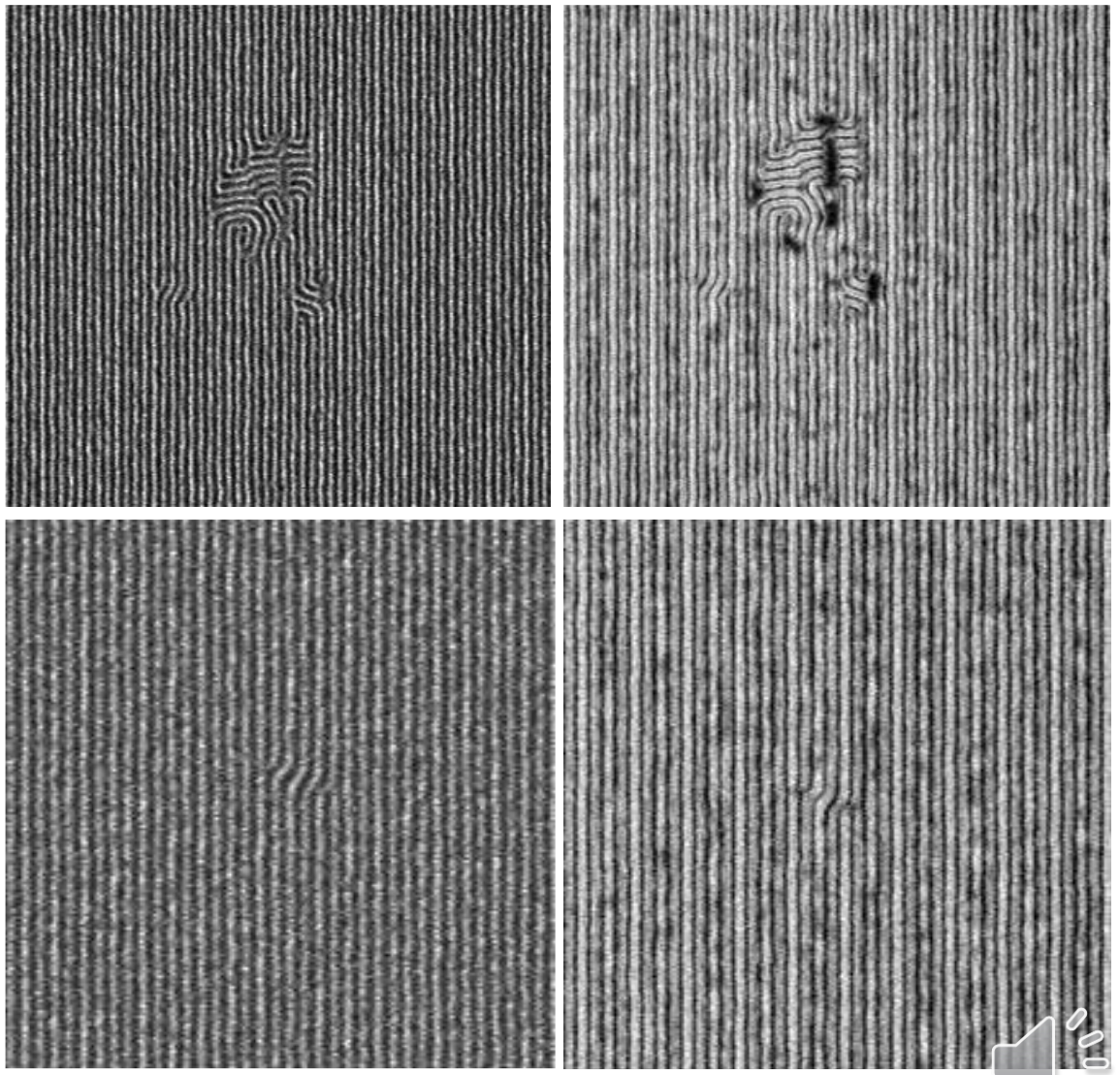
Confidential

CAPABILITY FOR FINE DEFECT REVIEW AND CLASSIFICATION

The higher resolution mode allows for finding

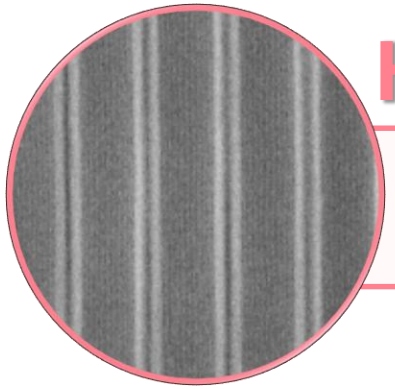
- Large assembly defects
- Smaller dislocations (e.g. 3)

Without etching PS into TiN substrate



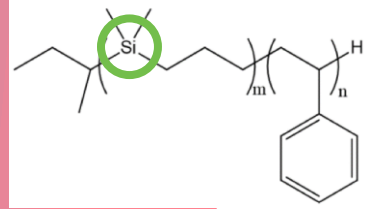
Confidential

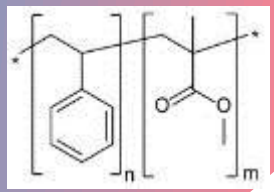
DSA DEVELOPMENTS



Highχ (L_0<20nm)

- **Mandatory for sub N5 L&S**





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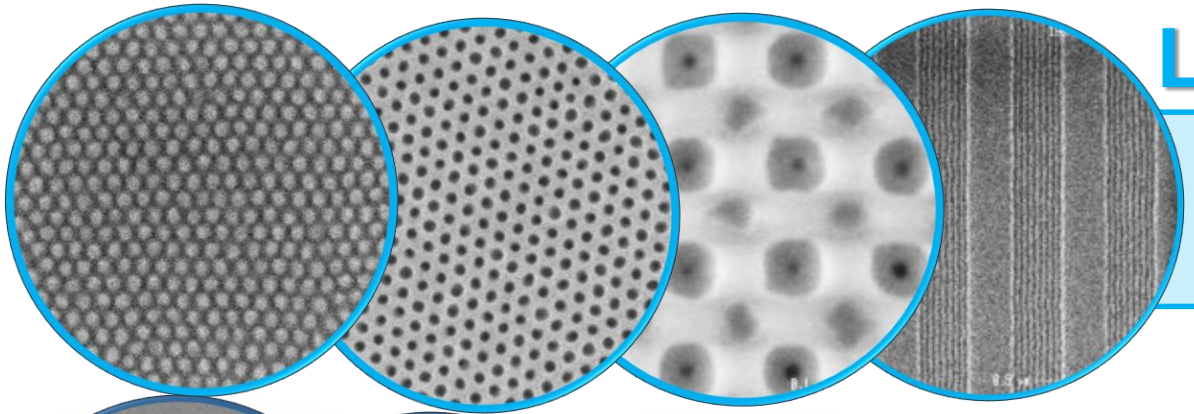
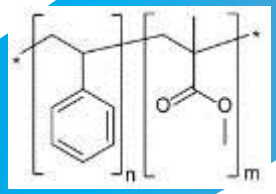
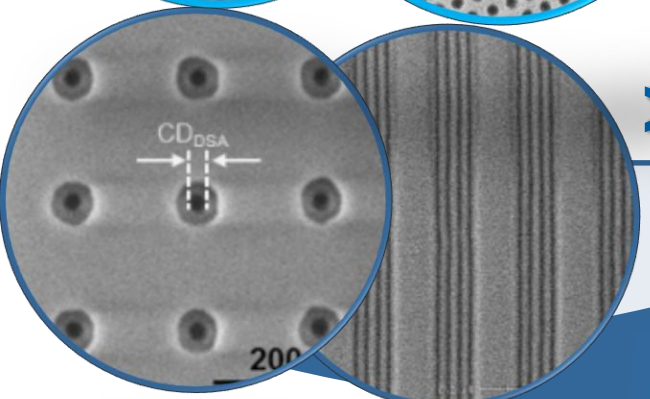


L22 (PS-b-PMMA)

- **Contact : Suitable down to N5**
- L&S : scalable down to N7
- Other application : sensors surface





>L38 (PS-b-PMMA)

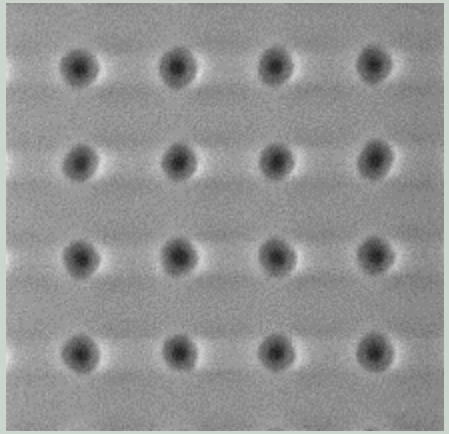
- **1st Gen DSA materials**
- Main application : contact/via
- Other application : sensors - surface

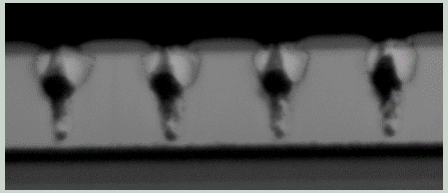
Process Development

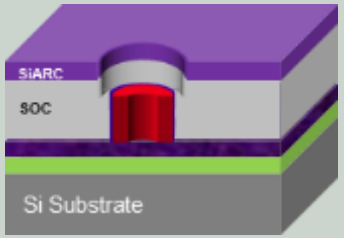
Process ecosystem

CONTACT FOR N10 VIA0 PATTERNING

SiARC/SOC *Organic template*



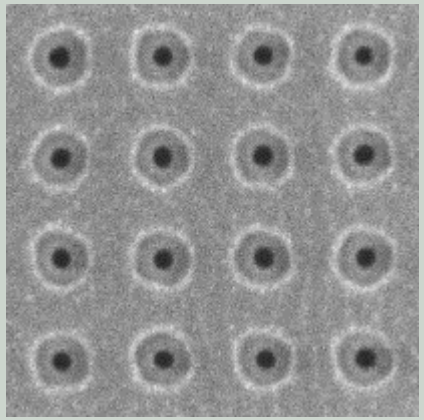


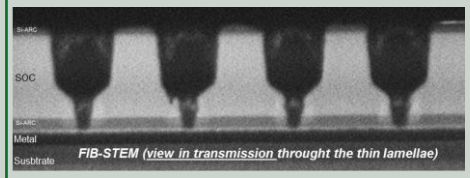


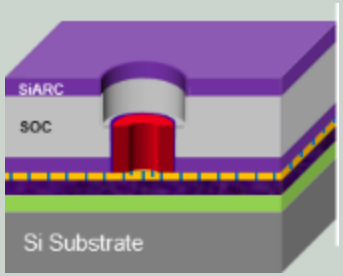
Guide template:
CD $_{guide}$ = 40.5 nm
CDU-3σ$_{guide}$ = 4.0nm

DSA:
CD = 17.2nm
CDU-3σ = 1.3nm
HOY = 100%
Planar: OK
Residue 3σ = 3.9nm
Rework : NO

SiARC/SOC *Embedded NL*



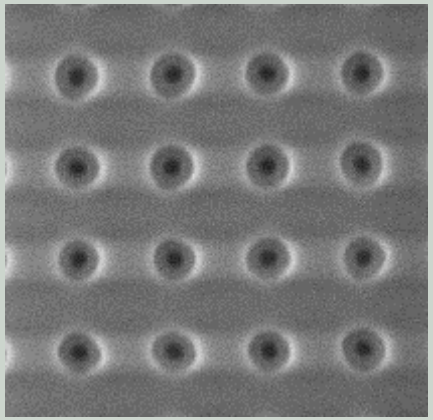


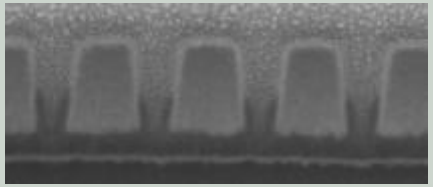


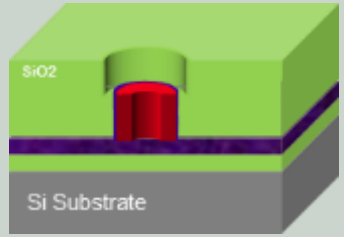
Guiding template:
CD $_{guide}$ = 50nm
CDU-3σ$_{guide}$ = 4.6nm

DSA:
CD = 22nm
CDU-3σ = 1.4nm
HOY = 100%
Planar OK
Residue 3σ = 0.6nm
Rework: NO

Silicon Oxide *Inorganic template*







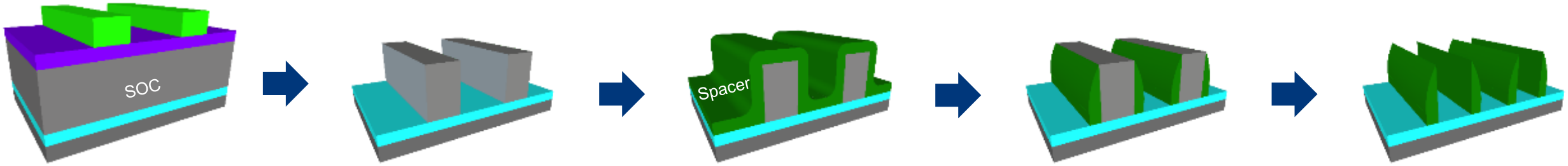
Guiding template:
CD $_{guide}$ = 40nm
CDU-3σ$_{guide}$ = 4.6nm

DSA:
CD = 17.6 nm
CDU-3σ = 1.4nm
HOY = 100%
Planar OK
Residue NA
Rework: OK

Several process options available for Contact hole integration

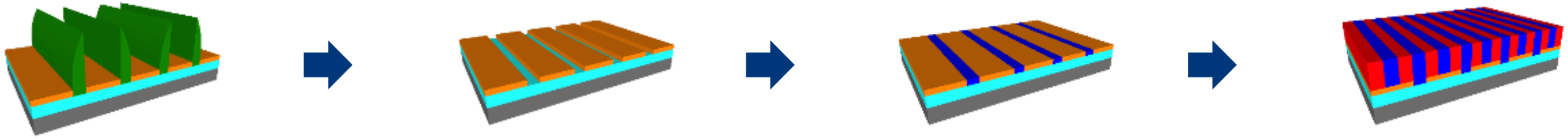
ADVANCED L&S PROCESS : “ACE” CONCEPT CEA-ARKEMA patented

1st part: SADP PROCESS



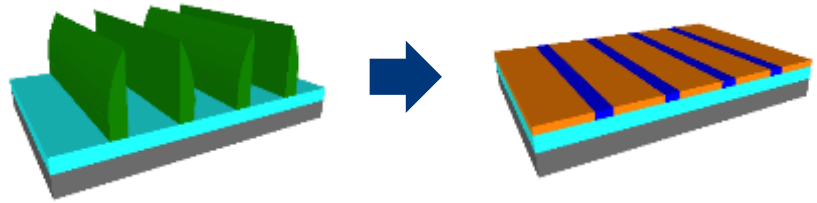
Lithography → Mandrel etch → Spacer deposition → Spacer etch → Mandrel pull

2nd part: DSA PROCESS ACE



Deposition of neutral layer → Spacer removal by wet etching → Selective grafting of guiding material → BCP self-assembly

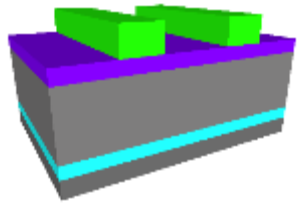
ACE PROCESS ADVANTAGES

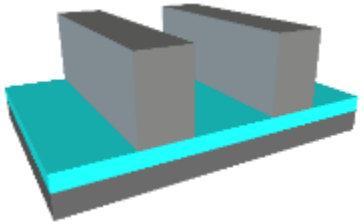


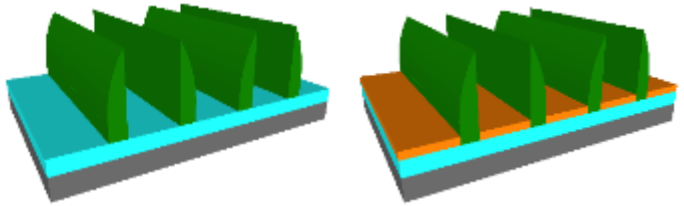
Process	BCP L_0 (nm)	Lithography guide period (nm) MF2	MF3	MF4	MF5	CD guide (nm)
LiNe & SMART	30	60	90	120	150	15
	18	36	54	72	90	9
	14	28	42	56	70	7
ACE	30	120	180	240	300	15
	18	72	108	144	180	9
	14	56	84	112	140	7

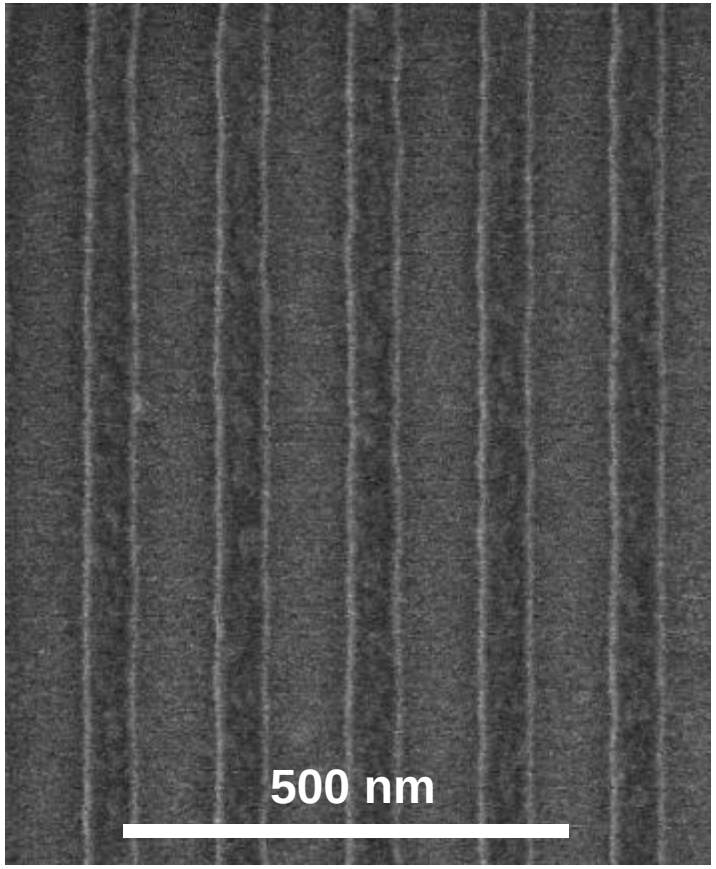
- Reduce multi-patterning scheme for SAxP strategy
- Support EUV insertion
  - Allow low Multiplication factors
  - Mitigate LER
  - Relax masks issues for clear field levels

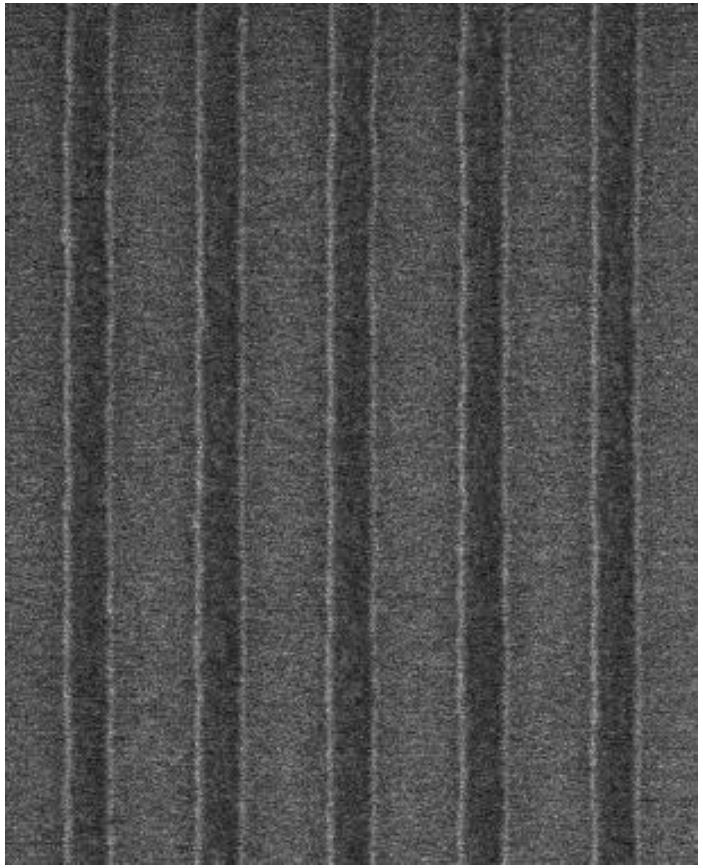
SPACER PATTERNING RESULTS

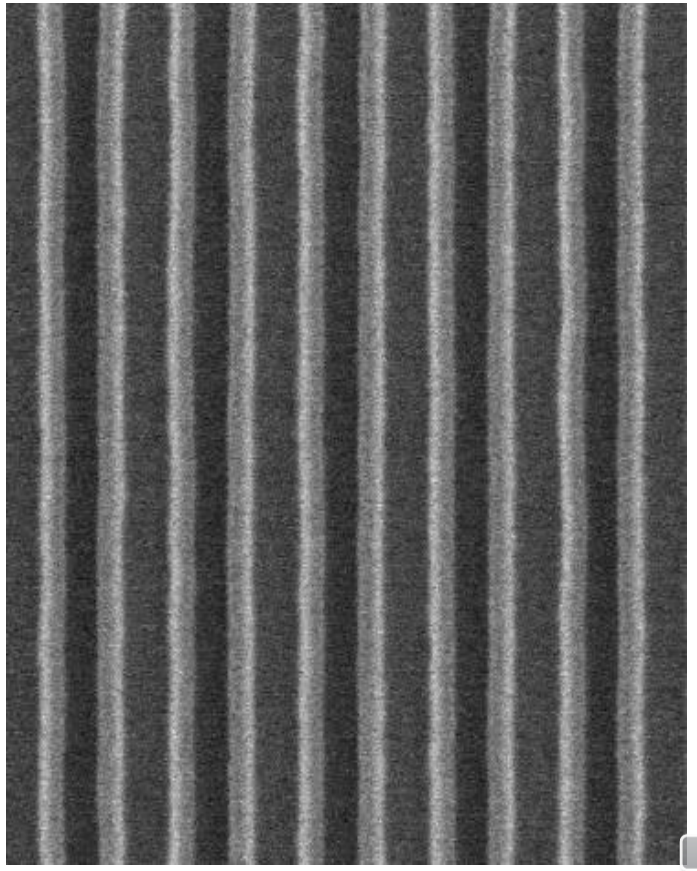




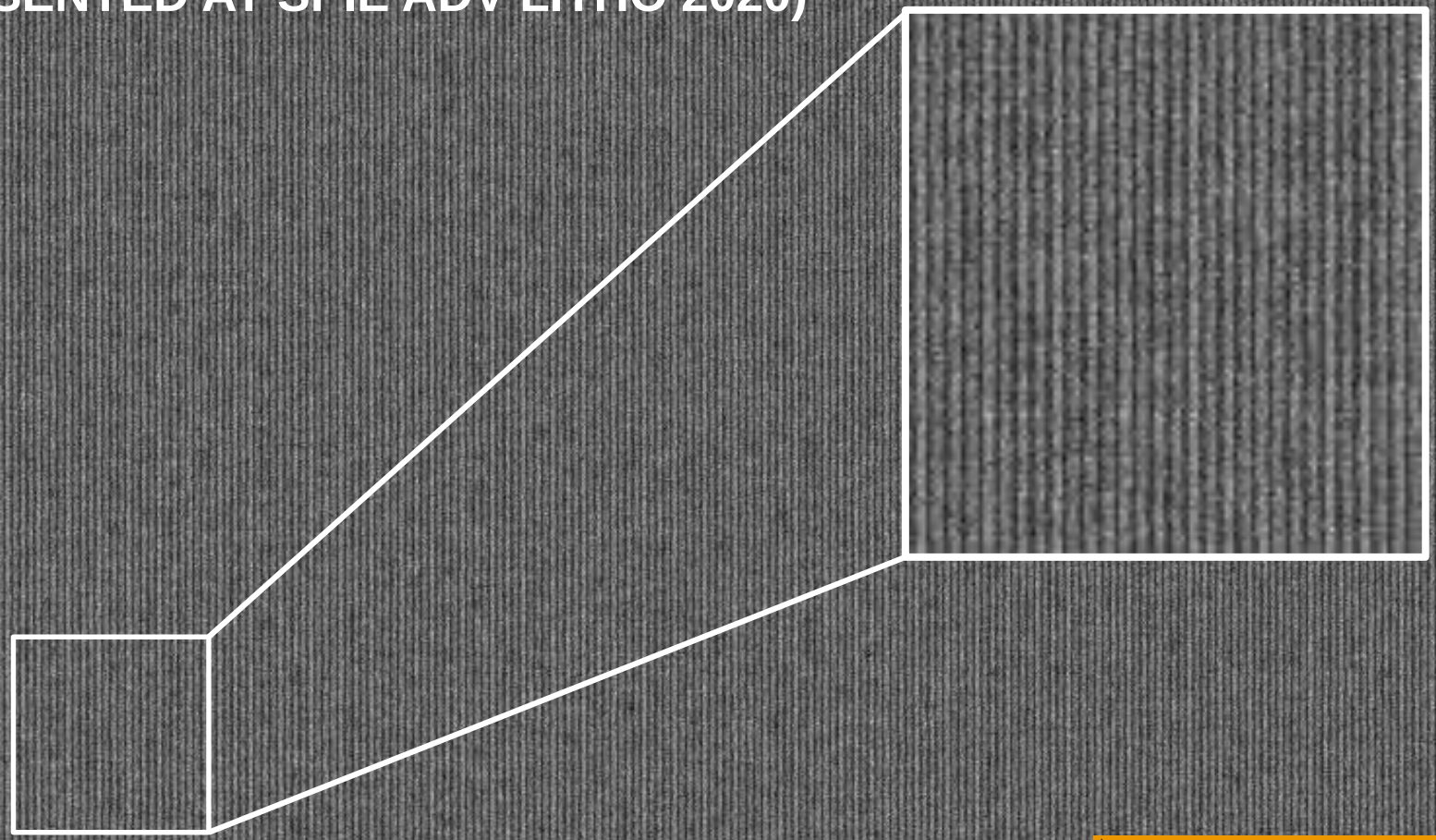


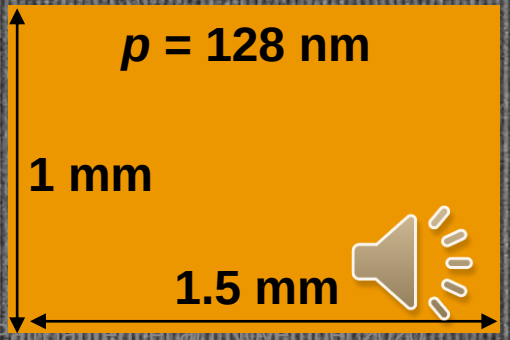






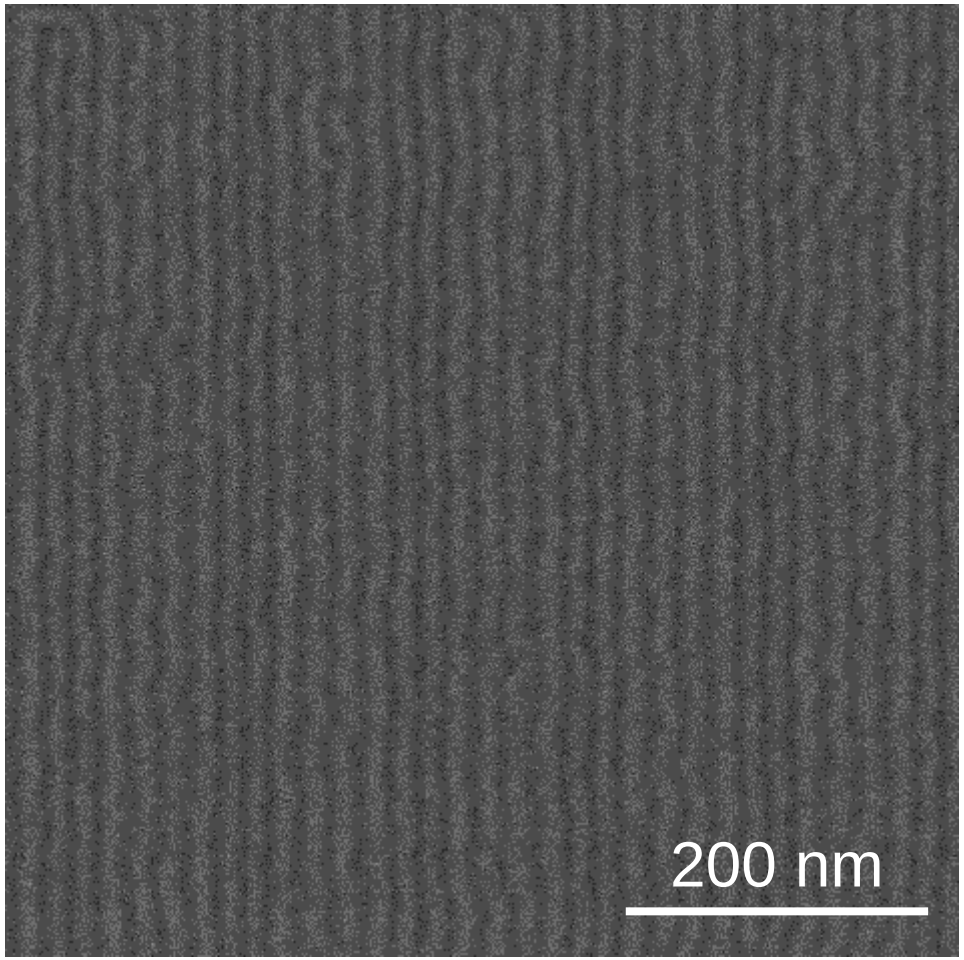
DSA OF L_0 = 31.5 NM, MF = (2,2)
(RESULT PRESENTED AT SPIE ADV LITHO 2020)

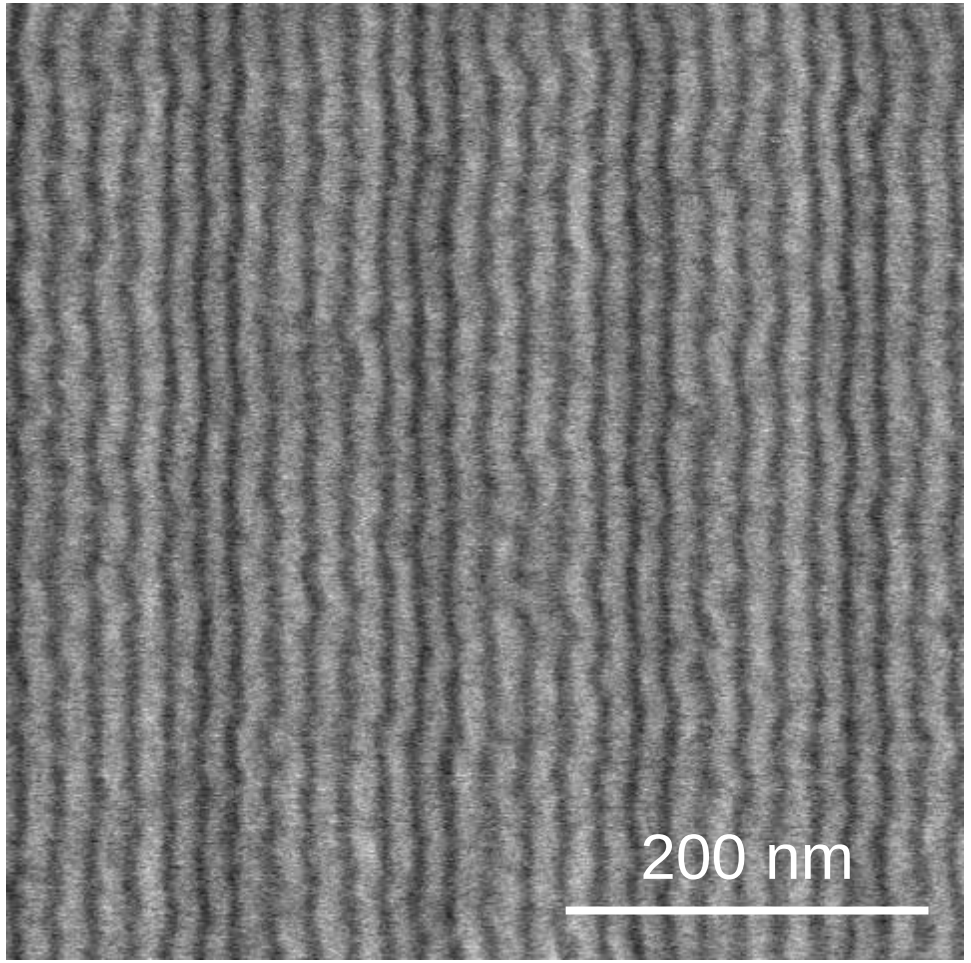




At least **10 µm x 10 µm without defects**

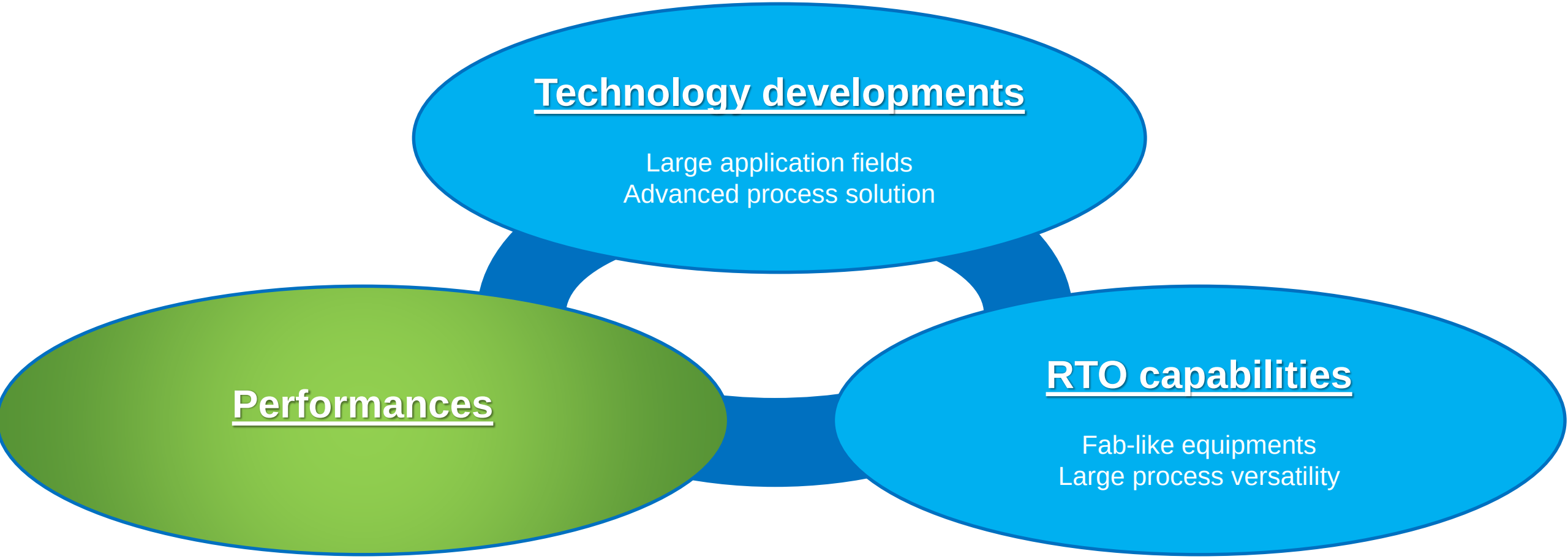
DSA OF MODIFIED HIGH-X PS-*B*-PMMA (L_0 = 18.5 NM)





First results of DSA of high-χ PS-*b*-PMMA (L_0 = 18.5)

FOCUS 3 – RTO PRODUCTION EFFICIENCY



RTO PLATFORM STRENGTHS

1. Fab flexibility & efficiency management

- Regular lot shuttle start
- Steady maturity increase
- Cycle time focus

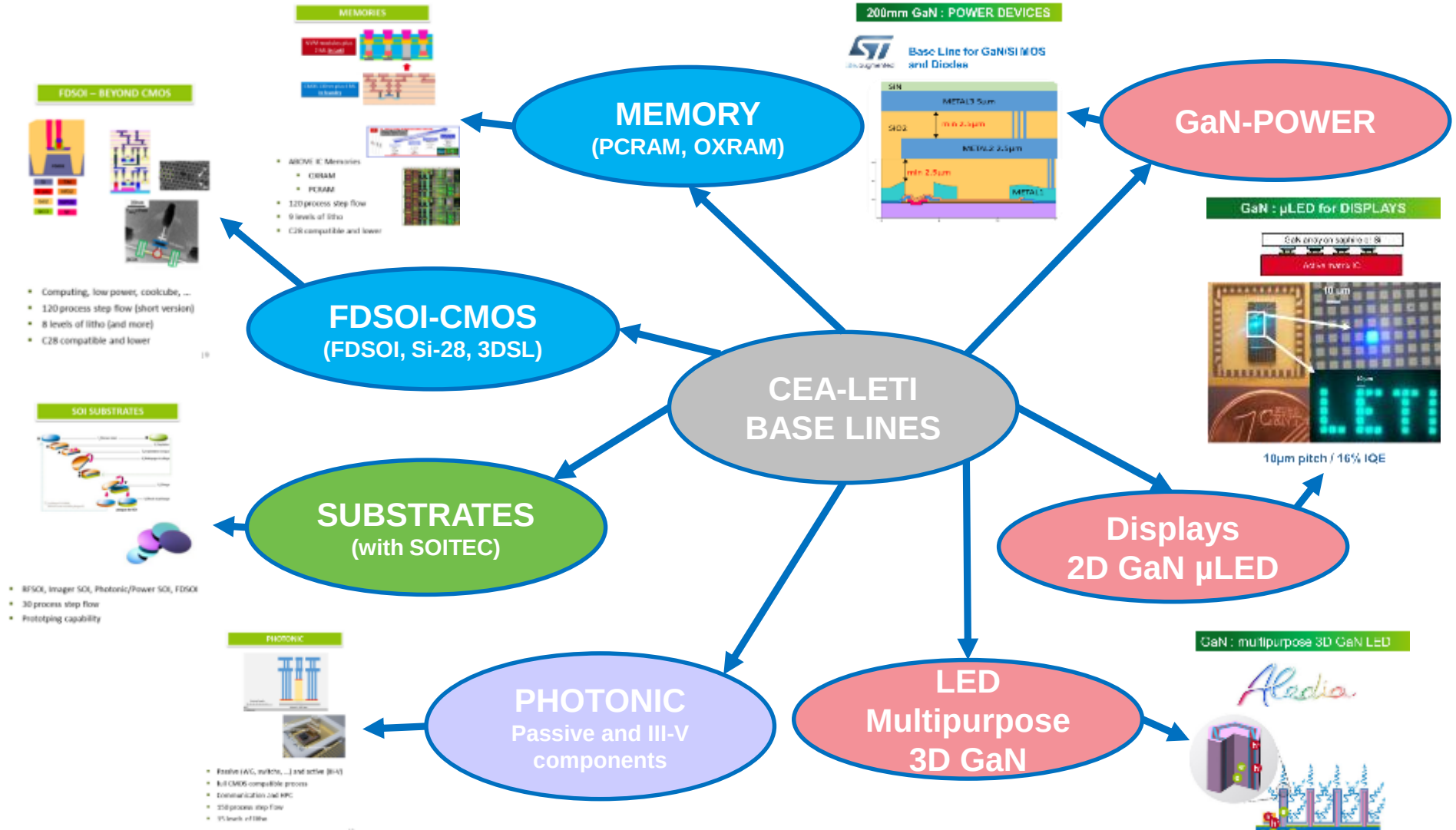
Cycle time
Maturity

2. MPW platform

- Confidentility
  - Validate private design Ips
- Fast transfer opportunity
  - Direct learning on production-like platform

Confidentiality
Transfer capability

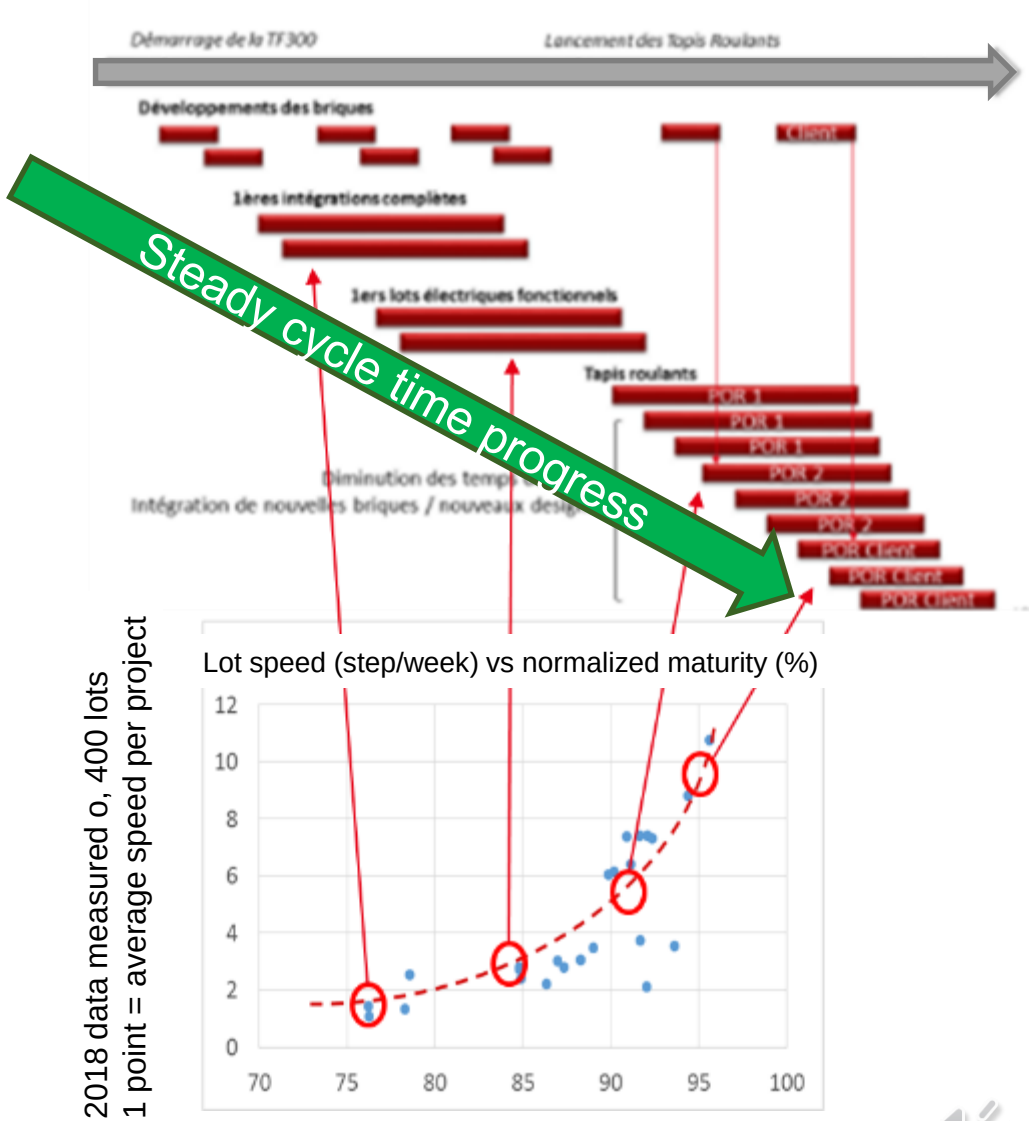
OPTIMIZE R&D EFFICIENCY ON CORE TECHNOLOGY ROUTES



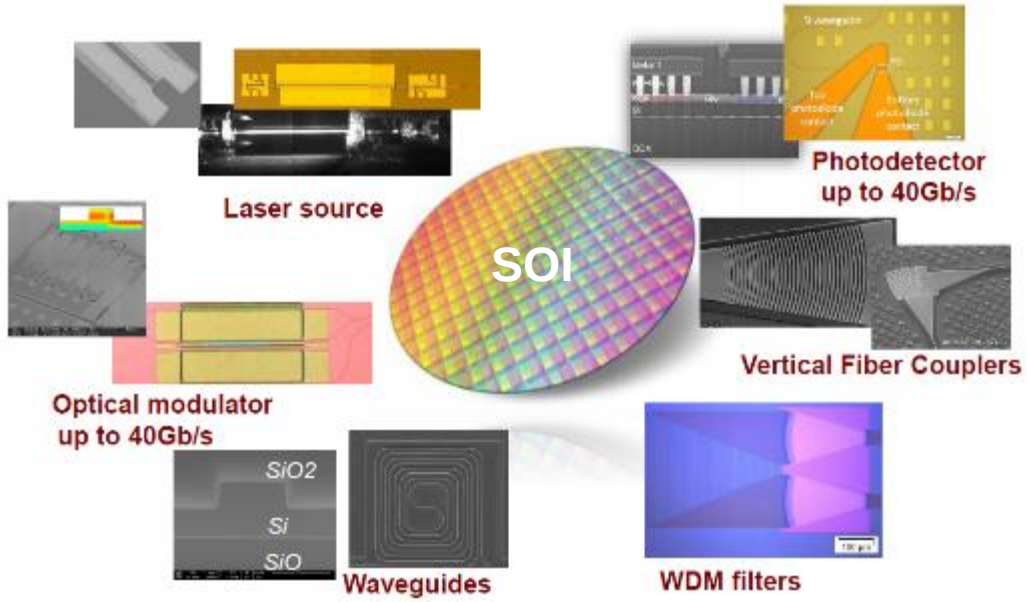
TECHNOLOGY BOOSTER : SHUTTLE LOT CONCEPT

- **Shuttle lot concept**
  1. Recurrent lot start on core route technology
  2. Optimize engineering on key process module

- **Advantages**
  1. Regular lot start
     - Mature process flow maturity
     - Progressive data extraction results
     - Easy way to adapt work plan
  2. Reduce cycle time engagement by
     → Raising process maturity on full process flows
     → Pushing in-line controls
  3. Maintain engineering on critical R&D blocks



SILICON PHOTONICS: OPENING OPPORTUNITIES

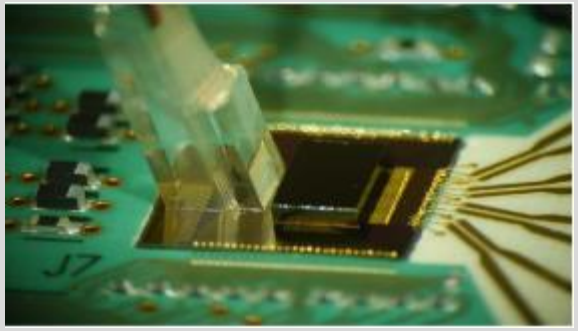


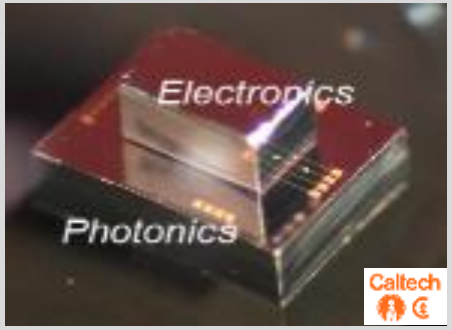
TOWARDS NEW APPLICATIONS

Advanced computing
Neuromorphic, reservoir et quantum

Optical sensors
Health, Environment, Automotive

3D Imaging & LIDAR
Indoor/outdoor automotive, drone, smartphone etc.



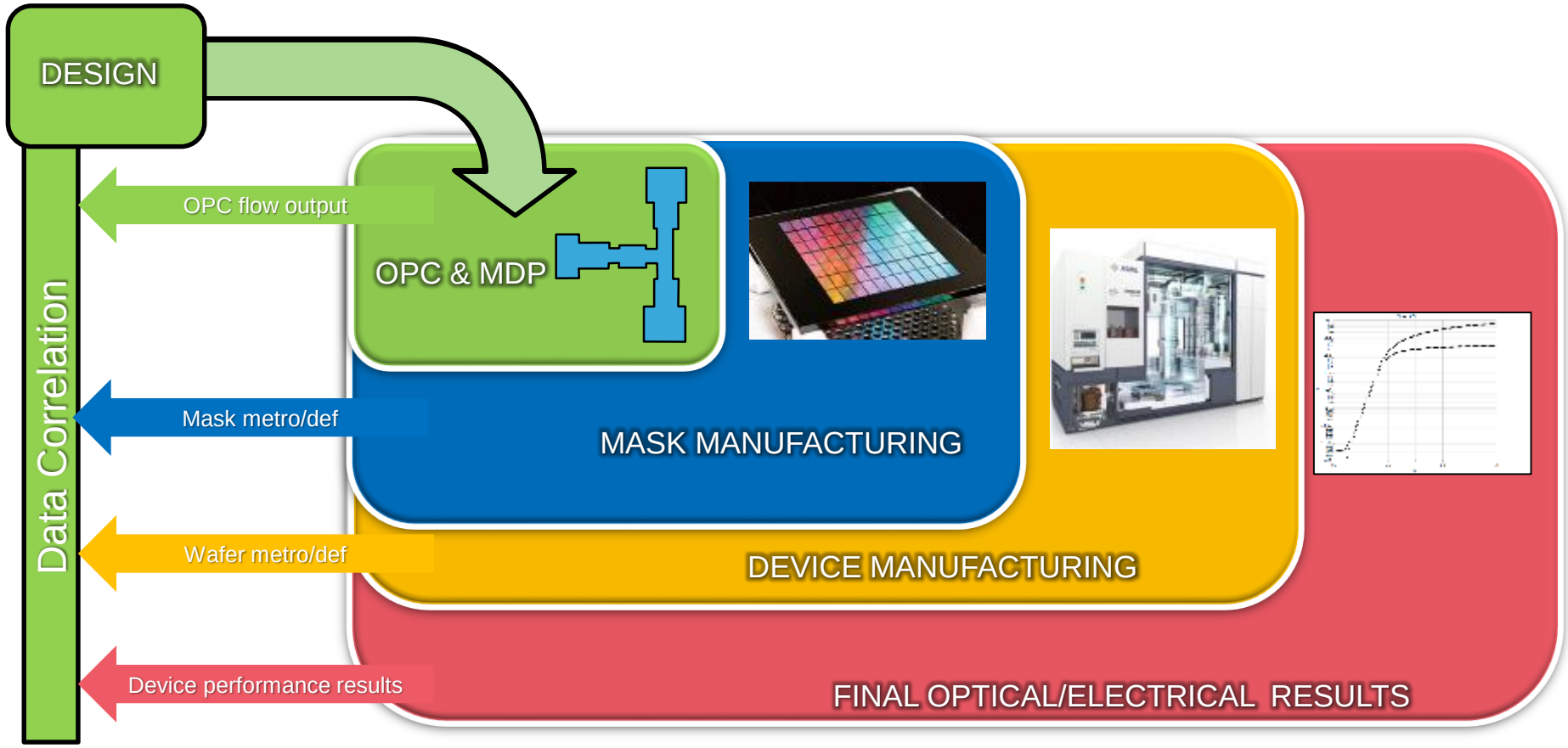


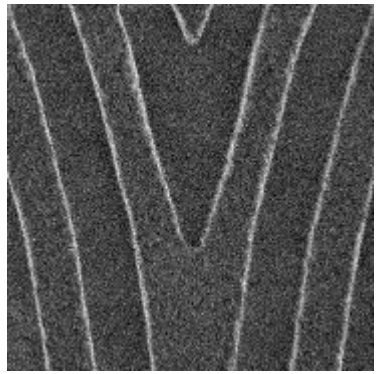
Computer Interconnections

PHOTONIC TECHNOLOGY PLATFORM

MULTI PROJECT WAFER
Silicon Photonics Offer

ECOSYSTEM DEVELOPMENT AROUND PATTERNING FOR PIC DEVICE





Photonics waveguide

AIMS
→ Optimize waveguide performance
→ Develop robust DKM
→ Rise maturity & cycle time

CONFIDENTIAL

OUTLINE

- **RTO ecosystem**
- **3 aspects on RTO efficiency parameters**
  - Fab capabilities
  - Technology development
    - CMP program
    - DSA patterning
  - Fab performances
- **Conclusions**

RTO EFFICIENCY

Technology development

Large application fields
Advanced process solution

Performances

Cycle time commitment
Constant maturity improvement

RTO capabilities

Fab-like equipments
Large process versatility

THE INNOVATION VIRTUOUS LOOP OF RTOs

Device test ?
Material ?
Process?

Substrate
CMOS
Power
LED
3D
Display
Photonique

Technology offer
Innovative solution
Shared NRE

Manufacturing
Cycle time
Technology maturity

Fab mission
Performance progress
Ready to transfer

Process flow
Module
Full block

Outcome

Demonstrator
Testchip
prototype

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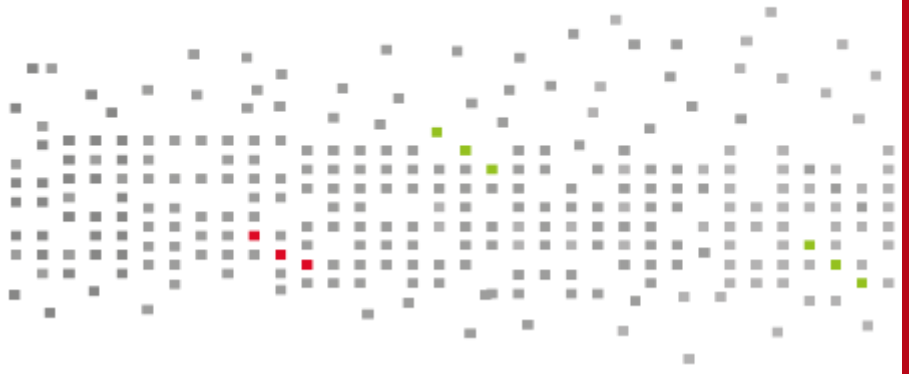
- Industrial partners : Applied Materials, SCREEN, TEL, ARKEMA, BREWER, ENTEGRIS, STmicroelectronics

- Special thanks : R Tiron, C Navarro, C Couderc,



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