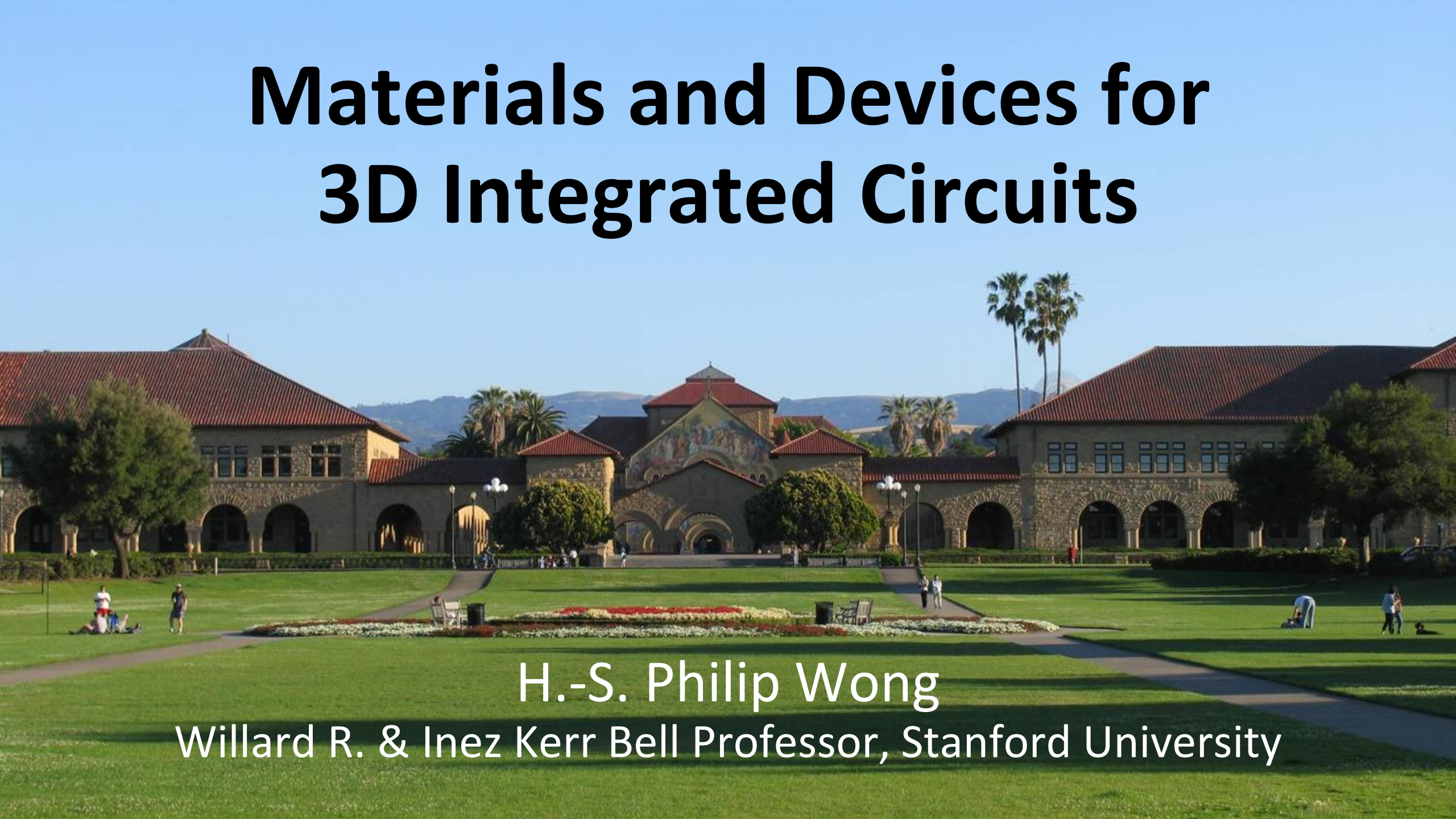
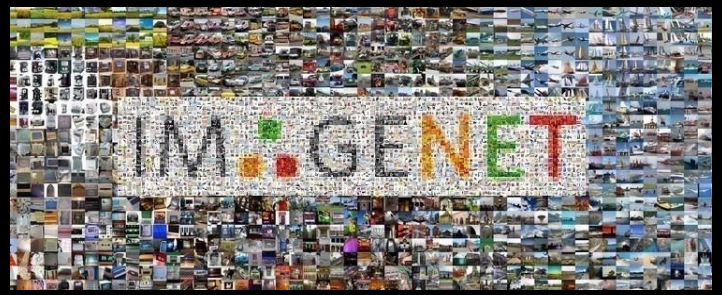
Materials and Devices for 3D Integrated Circuits



H.-S. Philip Wong
Willard R. & Inez Kerr Bell Professor, Stanford University

Photo by **Andrea Piacquadio** from **Pexels**


IMAGENET

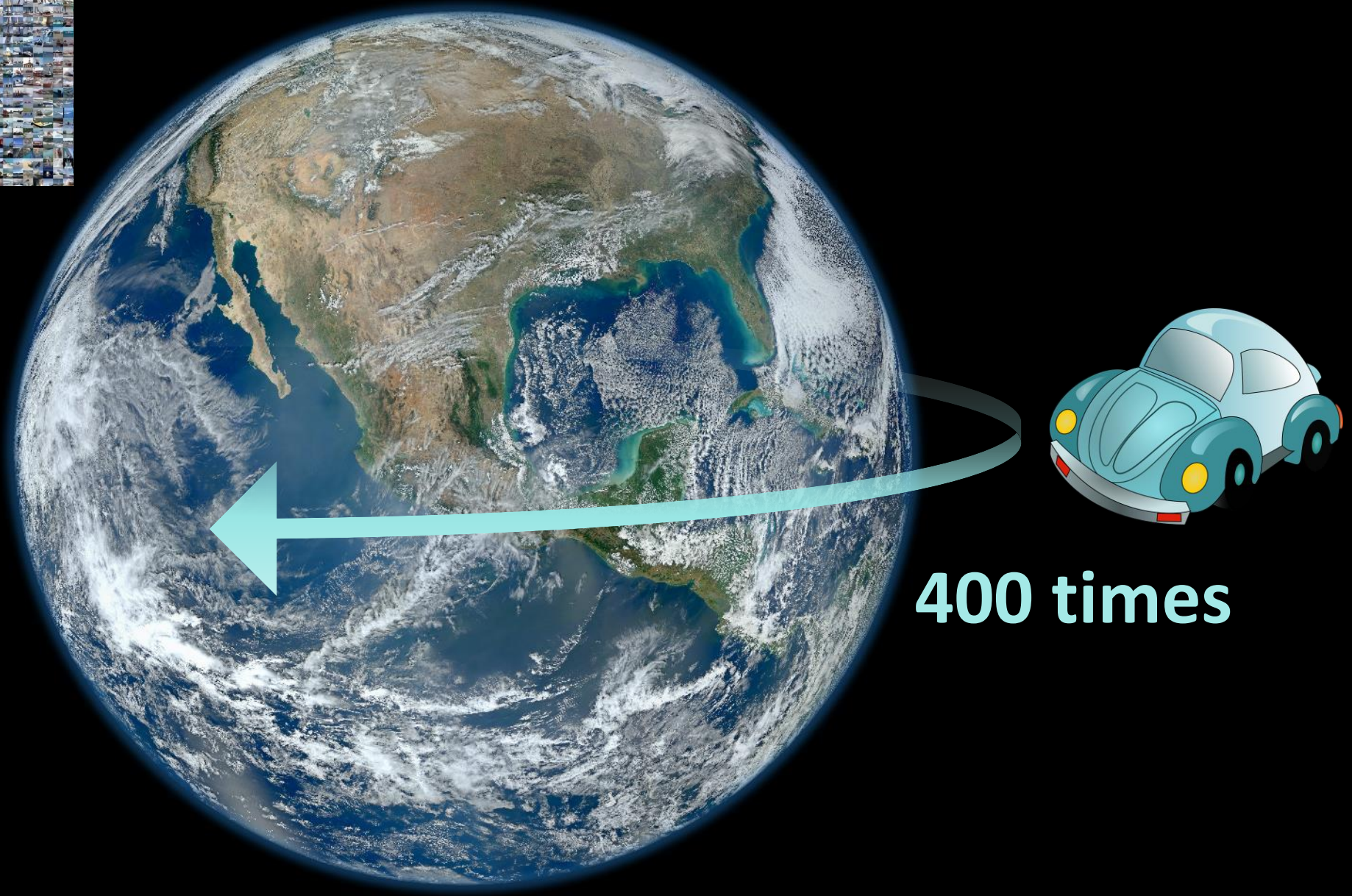
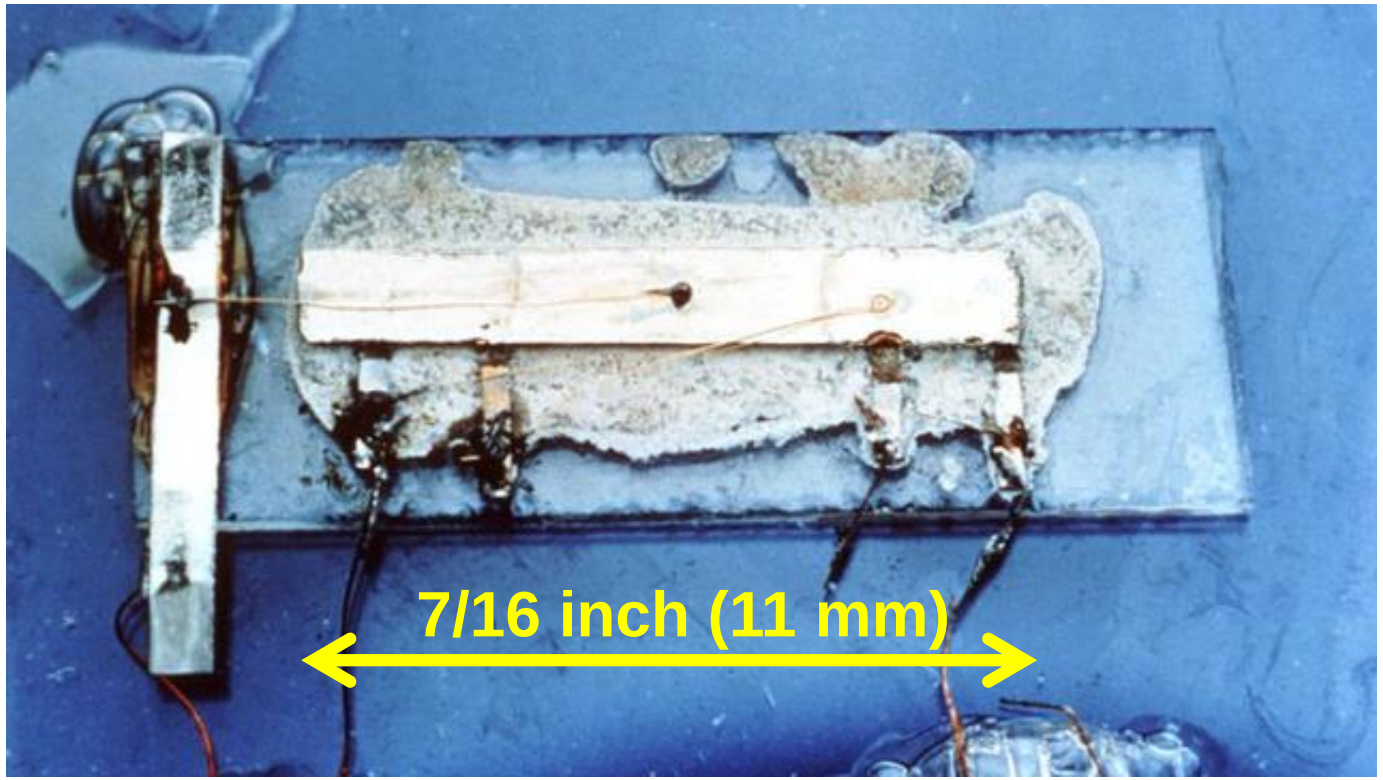
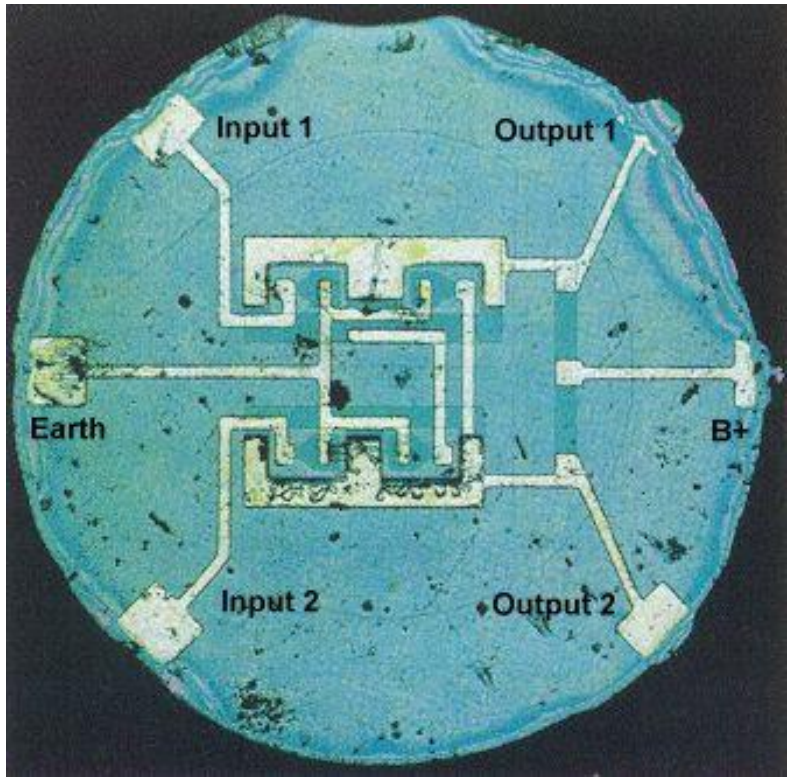

400 times

Photo by Akil Mazumder from Pexels

Integrated Circuit (IC, aka Semiconductor Chips)



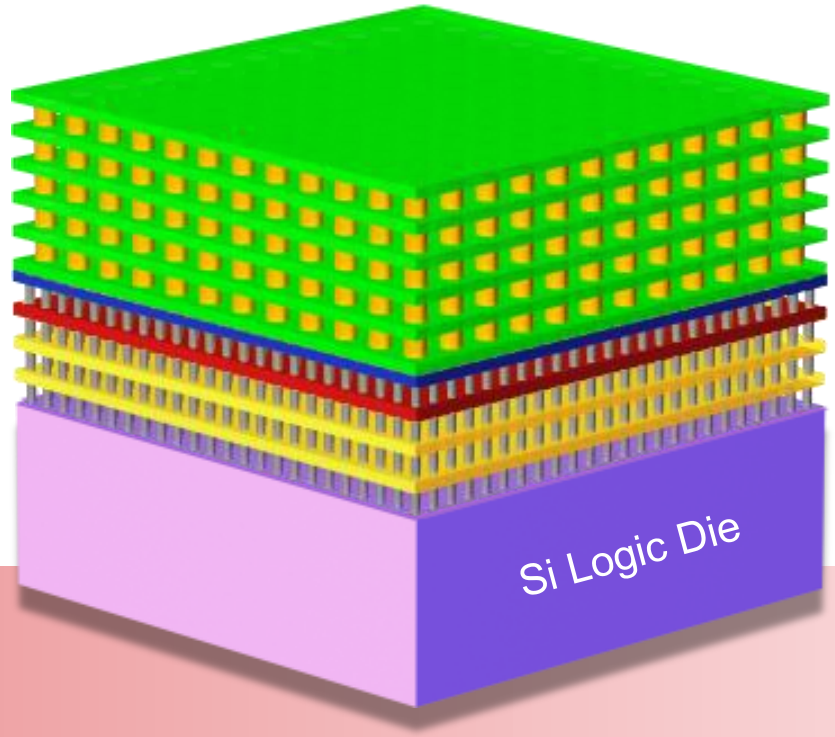


Jack Kilby, 1958

Robert Noyce, 1959

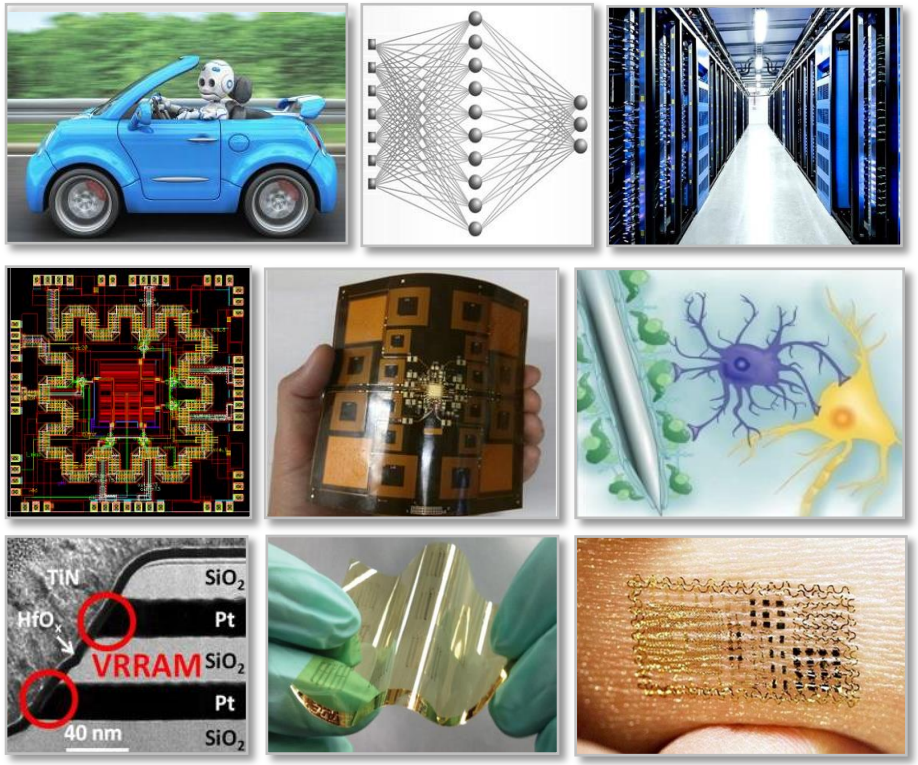
3D INTEGRATED CIRCUITS

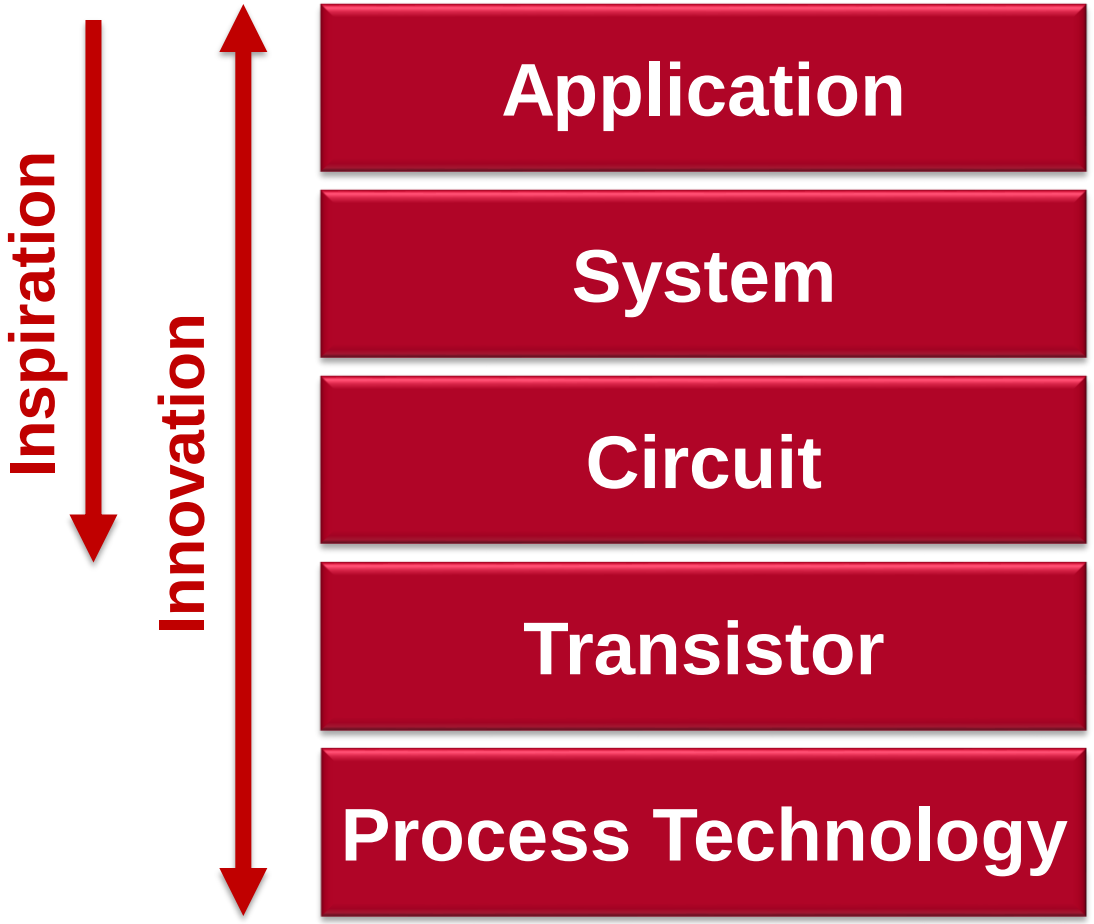
Transistors integrated with memory in **3D**



Stanford SystemX Alliance

SYSTEM-DRIVEN INNOVATION FOR THE 21ST CENTURY

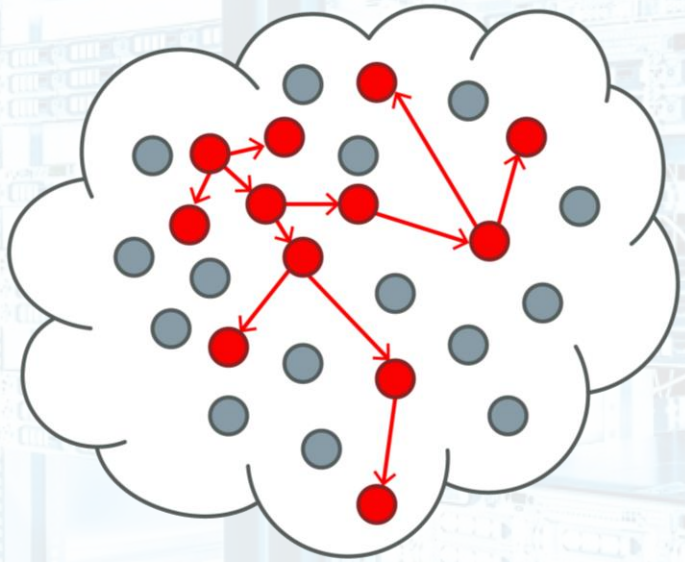




B. Murmann and H.-S. P. Wong, "Vision for a New Era in System Research," Stanford SystemX Alliance inaugural meeting, October 20, 2014

Big Data

Graph analytics



Machine learning

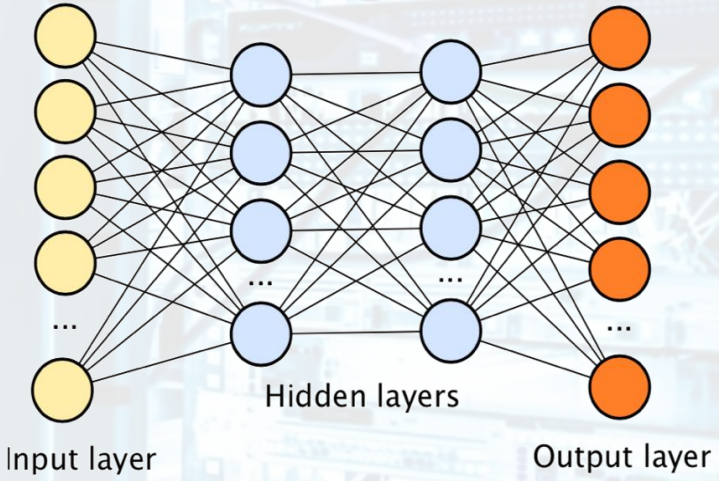
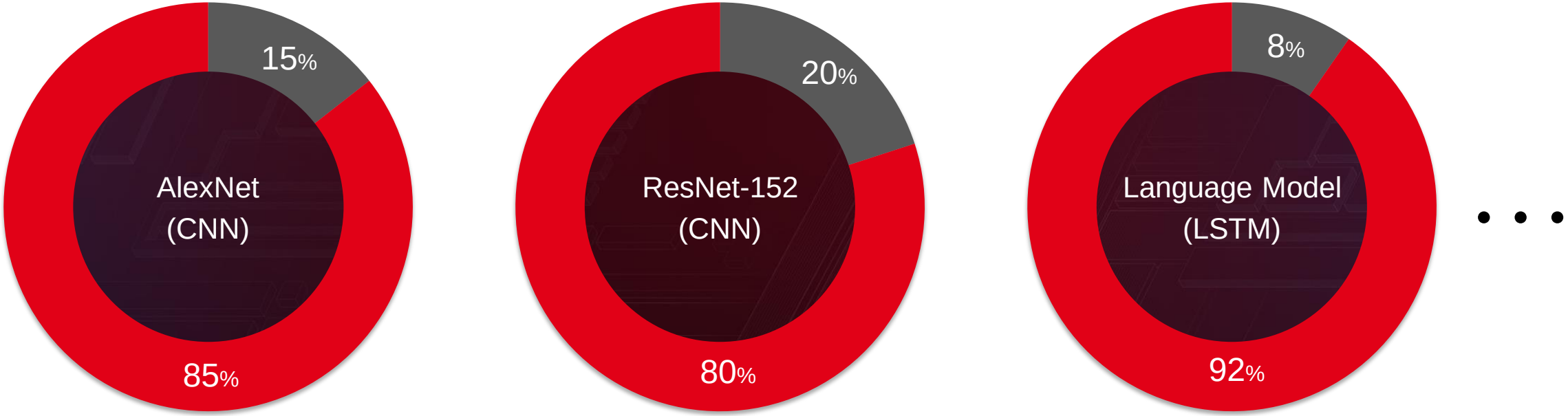


Image sources: Intel, bdtechtalks.com, Oracle, internetofbusiness.com

DATA MOVEMENT HITS THE MEMORY WALL

ABUNDANT-DATA APPLICATIONS: ENERGY MEASUREMENTS



Memory Compute

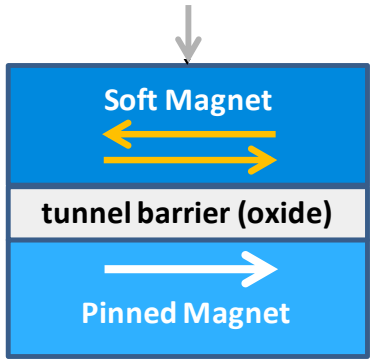
Deep Learning Accelerators

Source: S. Mitra (Stanford)

Intel performance counter monitors 2 CPUs, 8-cores/ CPU + 128GB DRAM

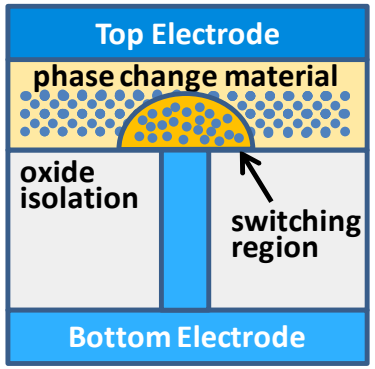
"NEW" MEMORIES FOR COMPUTE-MEMORY INTEGRATION

Random access, non-volatile, no erase before write, on-chip integration



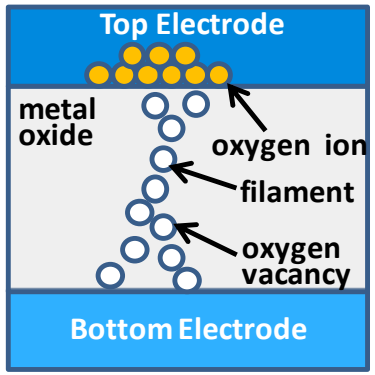
STT-MRAM

Spin **t**ransfer **t**orque **m**agnetic **r**andom **a**ccess **m**emory



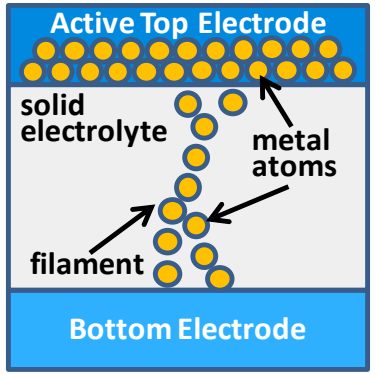
PCM

Phase **c**hange **m**emory



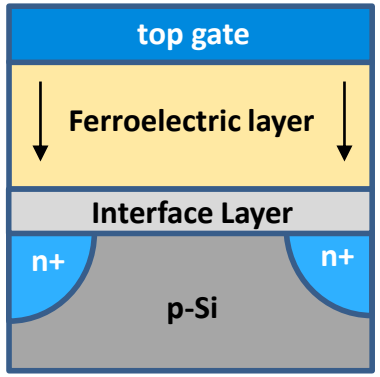
RRAM

Resistive switching **r**andom **a**ccess **m**emory



CBRAM

Conductive **b**ridge **r**andom **a**ccess **m**emory



FEFET

Ferro-**e**lectric **f**ield **e**ffect **t**ransistor

H.-S. P. Wong, S. Salahuddin, *Nature Nanotech.*, 2015

PRIMARY IMPORTANCE:

MEMORY CAPACITY AND BANDWIDTH

INVITED PAPER

The N3XT Approach to Energy-Efficient Abundant-Data Computing

This paper enables energy-efficient computing for transformative abundant-data applications through heterogeneous integration of energy-efficient logic devices immersed in dense nonvolatile memory, with fine-grained connectivity in a monolithic 3-D architecture.

By Mohamed M. Sabry Aly, Tony F. Wu, Andrew Bartolo, Yash H. Malviya, William Hwang, Gage Hills, Igor Markov, Mary Wootters, Max M. Shulaker, H.-S. Philip Wong, *Fellow IEEE*, and Subhasish Mitra, *Fellow IEEE*

Aly et al., *IEEE Proceedings* 2018

POINT OF VIEW

A Density Metric for Semiconductor Technology

By H.-S. PHILIP WONG
Stanford University, Stanford, CA 94305 USA
Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan
KEREM AKARVARDAR
Taiwan Semiconductor Manufacturing Company, San Jose, CA 95134 USA
DIMITRI ANTONIADIS
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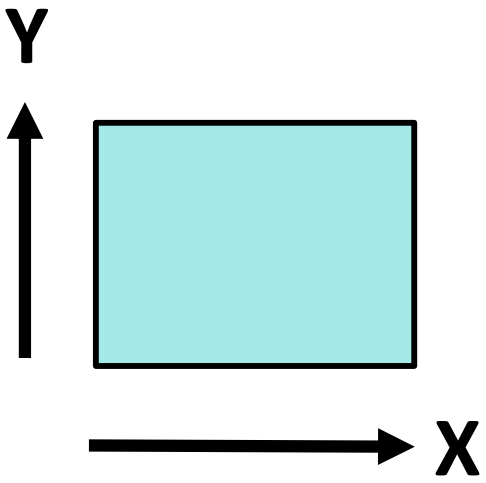
University of California at Berkeley, Berkeley, CA 94720 USA
CHENMING HU
University of California at Berkeley, Berkeley, CA 94720 USA
TSU-JAE KING-LIU
University of California at Berkeley, Berkeley, CA 94720 USA
SUBHASISH MITRA
Stanford University, Stanford, CA 94305 USA
JAMES D. PLUMMER
Stanford University, Stanford, CA 94305 USA
SAYEEF SALAHUDDIN
University of California at Berkeley, Berkeley, CA 94720 USA

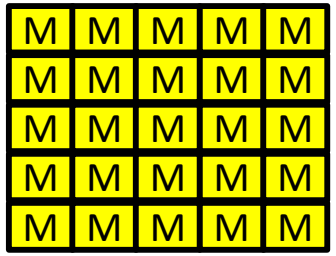
Wong et al., *IEEE Proceedings* 2020

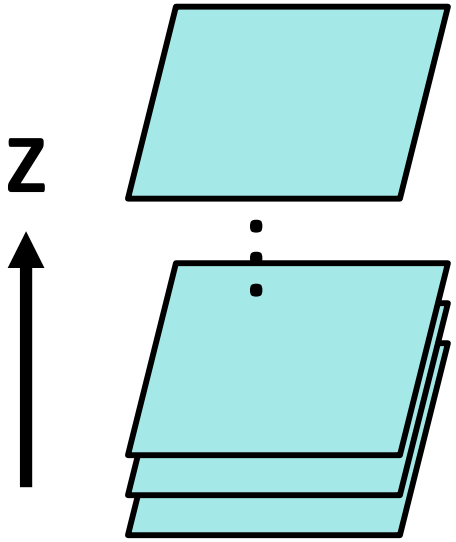
H.-S. P. Wong, *HotChips*, plenary paper (2019)

LARGE MEMORY CAPACITY:

X, Y, Z, M







- Two dimensional down scaling
- Store multiple bits per memory cell
- 3D layers

Inspired by Jian Chen (Western Digital), *IEDM Short Course*, 2019

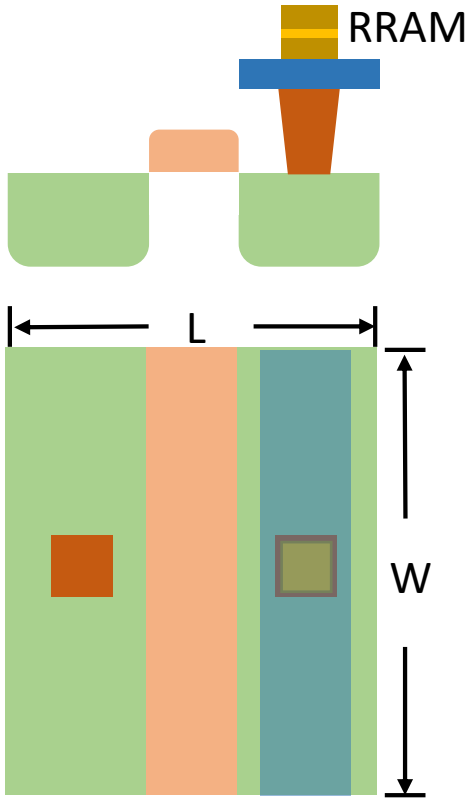
MEMORY CELL SIZE:

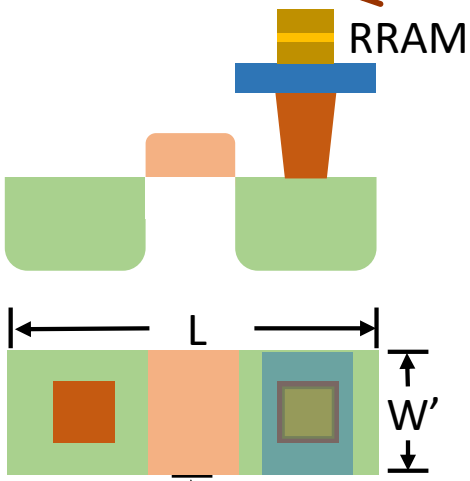
LIMITED BY TRANSISTOR SIZE

$\text{Area}_{\text{RRAM}} << \text{Area}_{\text{1T1R}}$

RRAM w/
Low programming
current

1T1R

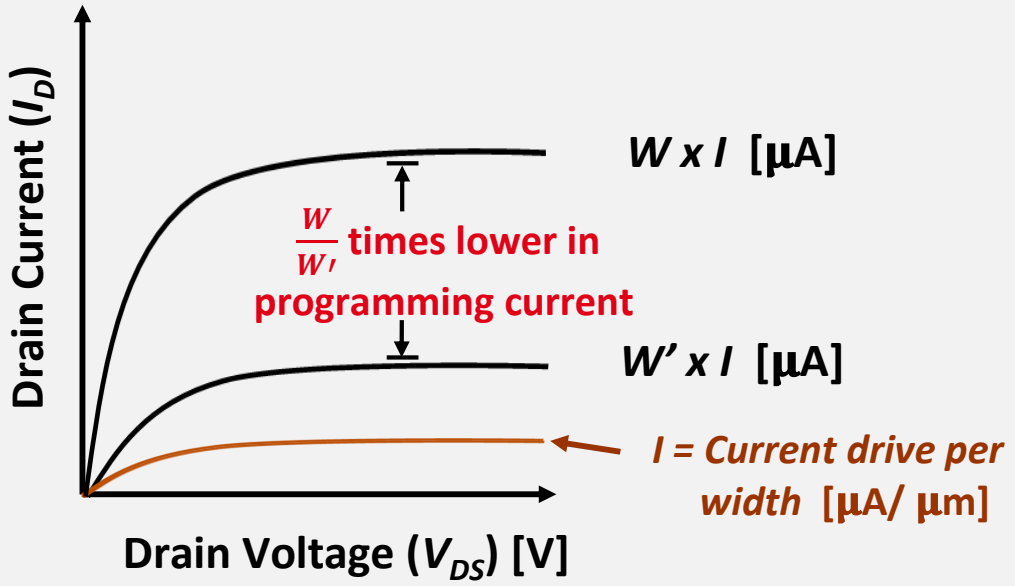




1T1R
Unit cell
Area: L x W

$\frac{W}{W'}$ times smaller area

Transistor current drive



HIGHER MEMORY CAPACITY: X, Y, Z, M

Low Programming Current

< 10 μA programming current to achieve dense layout

Multi-bit Cell

m-bit per cell = *m* times denser (not incl. peripheral circuitry)

Go 3D!

Stack up in the **vertical** direction

HIGHER MEMORY CAPACITY:

Low Programming Current

< 10 μA programming current to achieve dense layout

Multi-bit Cell

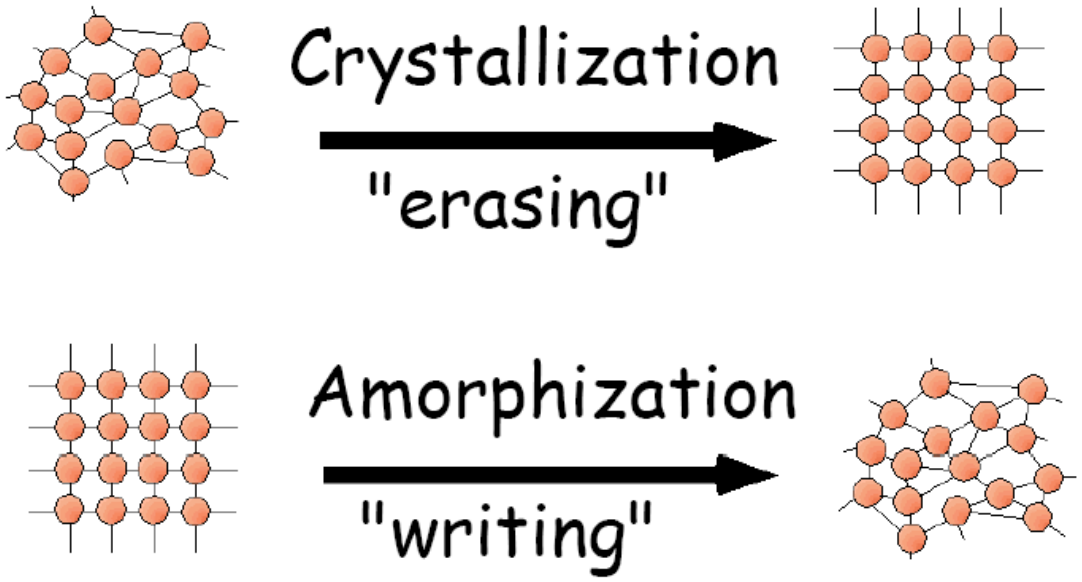
m-bit per cell = *m* times denser (not incl. peripheral circuitry)

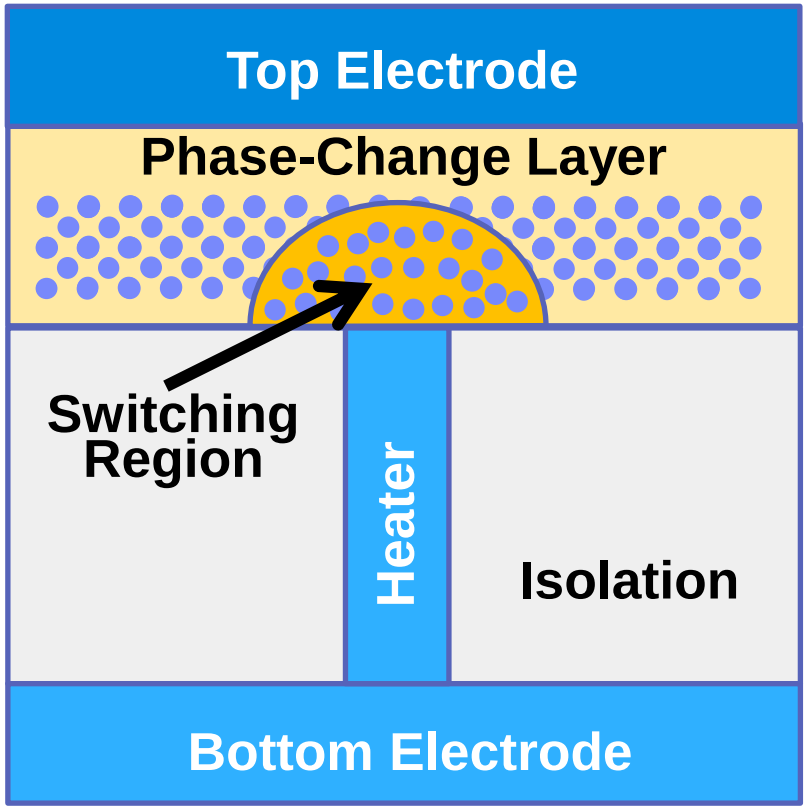
Go 3D!

Stack up in the **vertical** direction

PCM Switching Physics

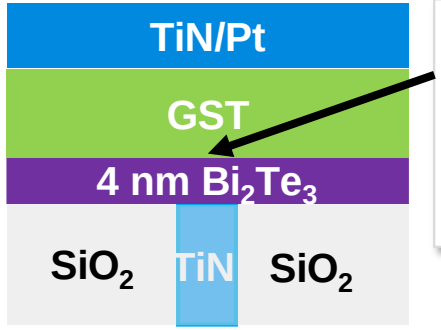
- Writing Mechanism: Current-induced Joule heating
- Amorphization (Reset): Melt and quench ($T > T_{Melt}$)
- Crystallization (Set): Anneal ($T > T_{crys}$)



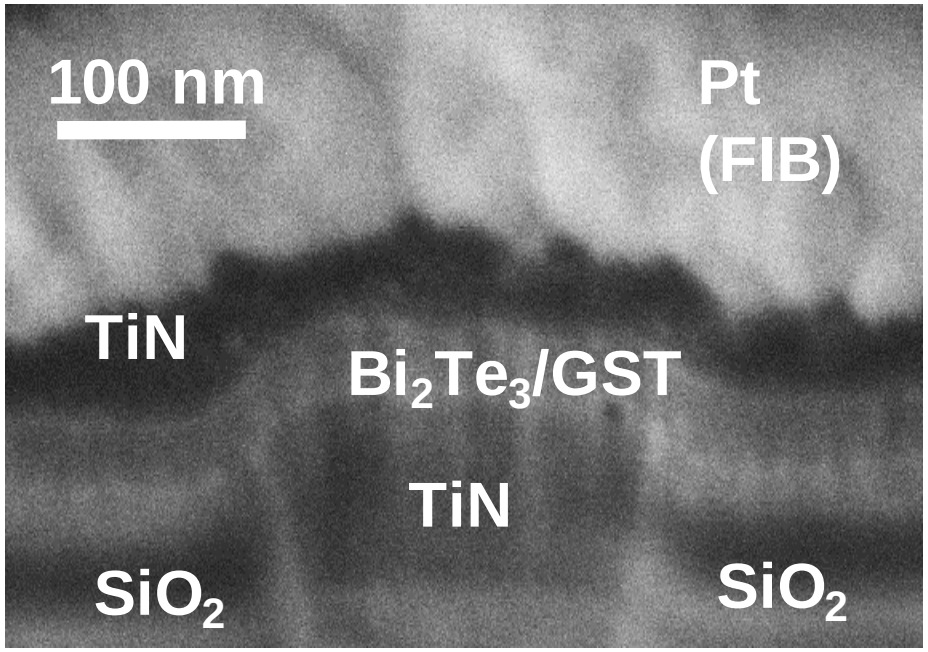


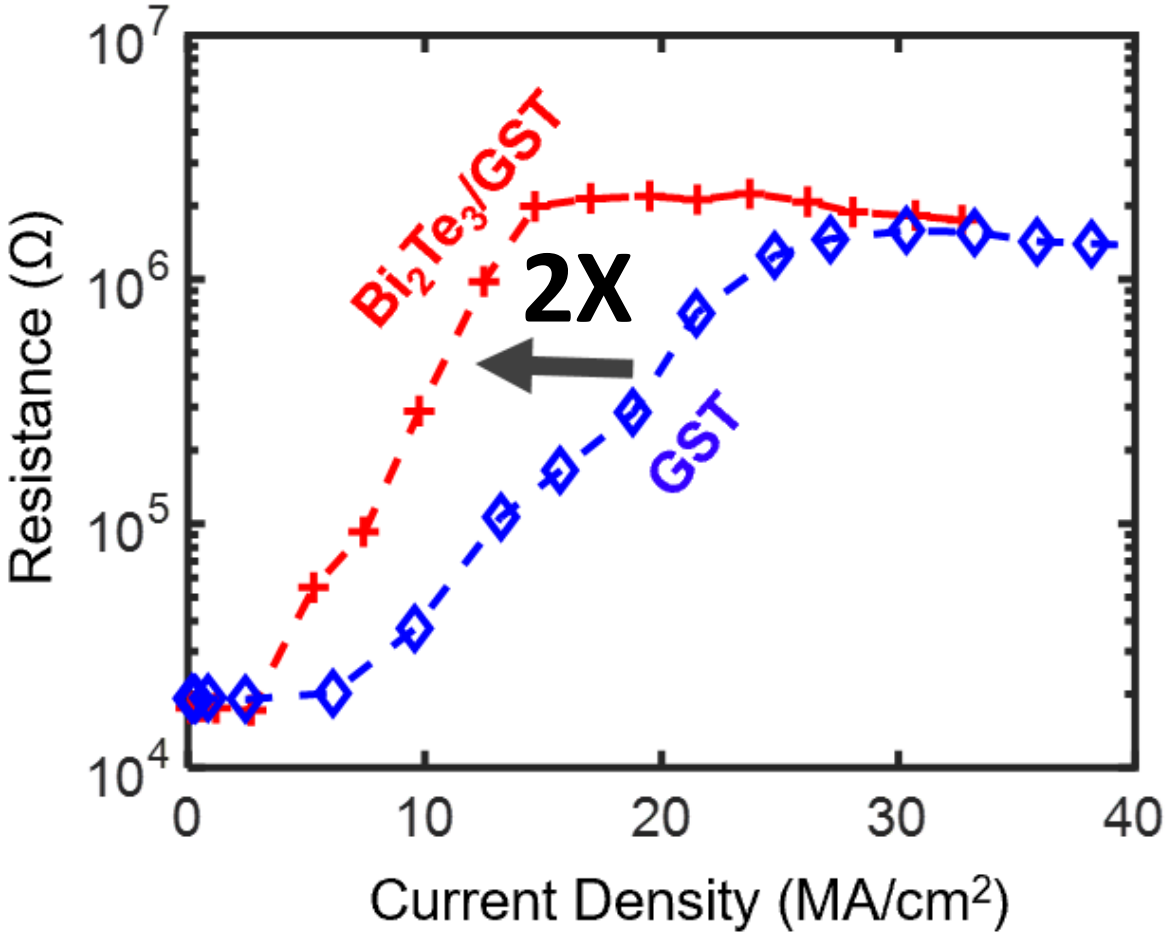
H.-S. P. Wong *et al.*, "Phase Change Memory," *Proc. IEEE* 2010.

PCM: INTERFACIAL THERMOELECTRIC LAYER (Bi_2Te_3) – REDUCES J_{RESET} BY 2X



Thermoelectric effect (thin Bi_2Te_3 layer) puts heat at desired location





A. Khan, H. Kwon, R. Islam, […], H.-S. P Wong, E. Pop, *IEEE EDL, in press (2020)*

HIGHER MEMORY CAPACITY:

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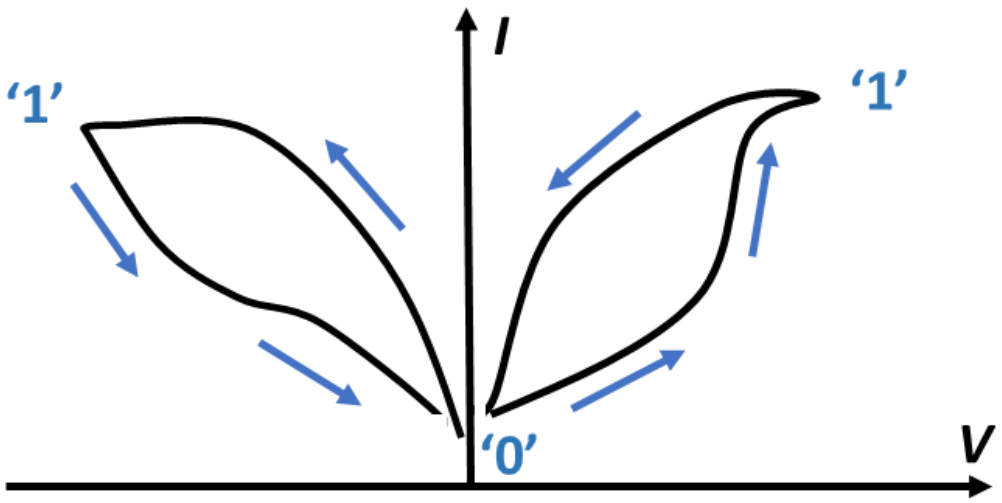
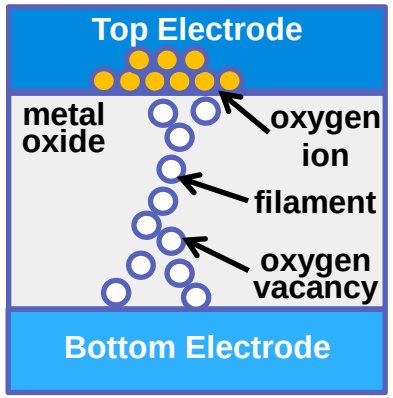
Go 3D!

Stack up in the **vertical** direction

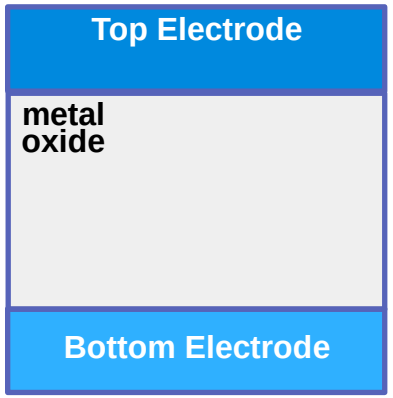
RRAM: Physics of Resistance Switching



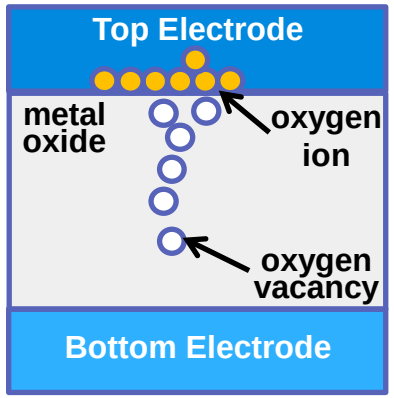
RRAM



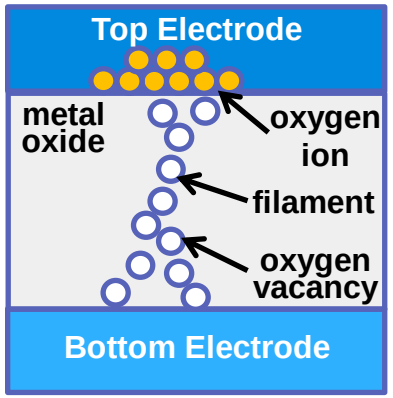
Pristine "0"



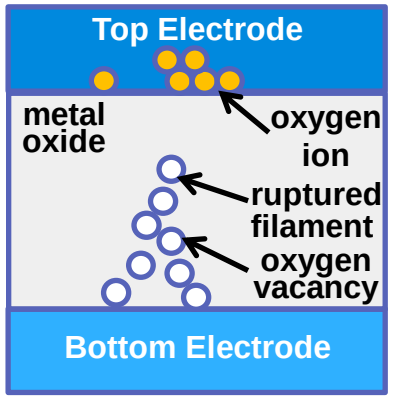
Set/forming



"1"

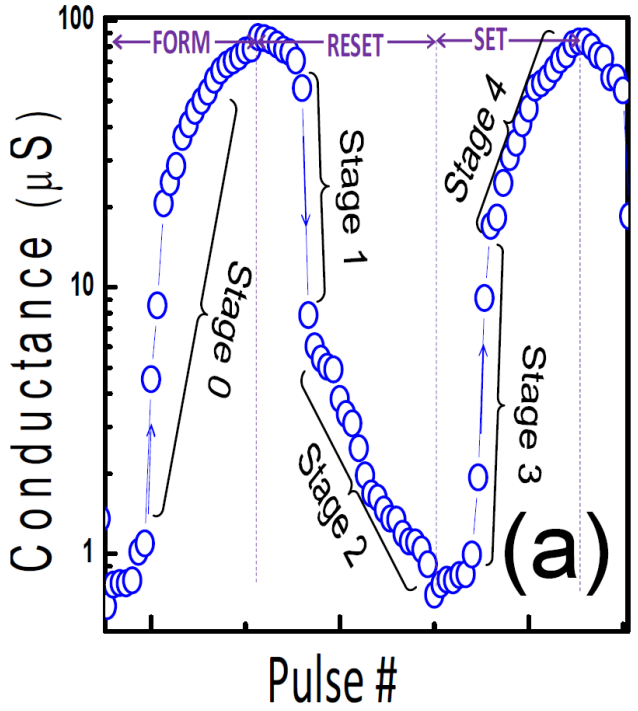


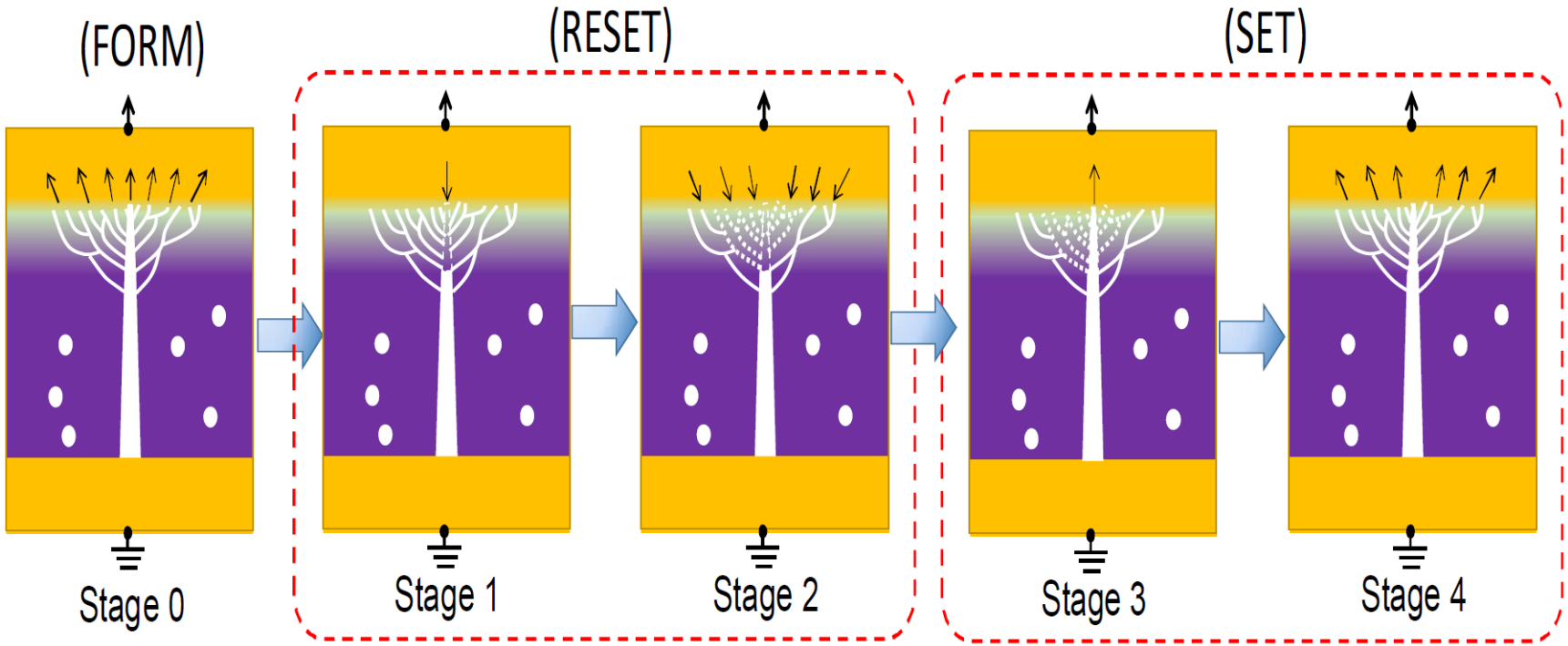
Reset "0"



H.-S. P. Wong, S. Salahuddin, *Nature Nanotech.*, 2015

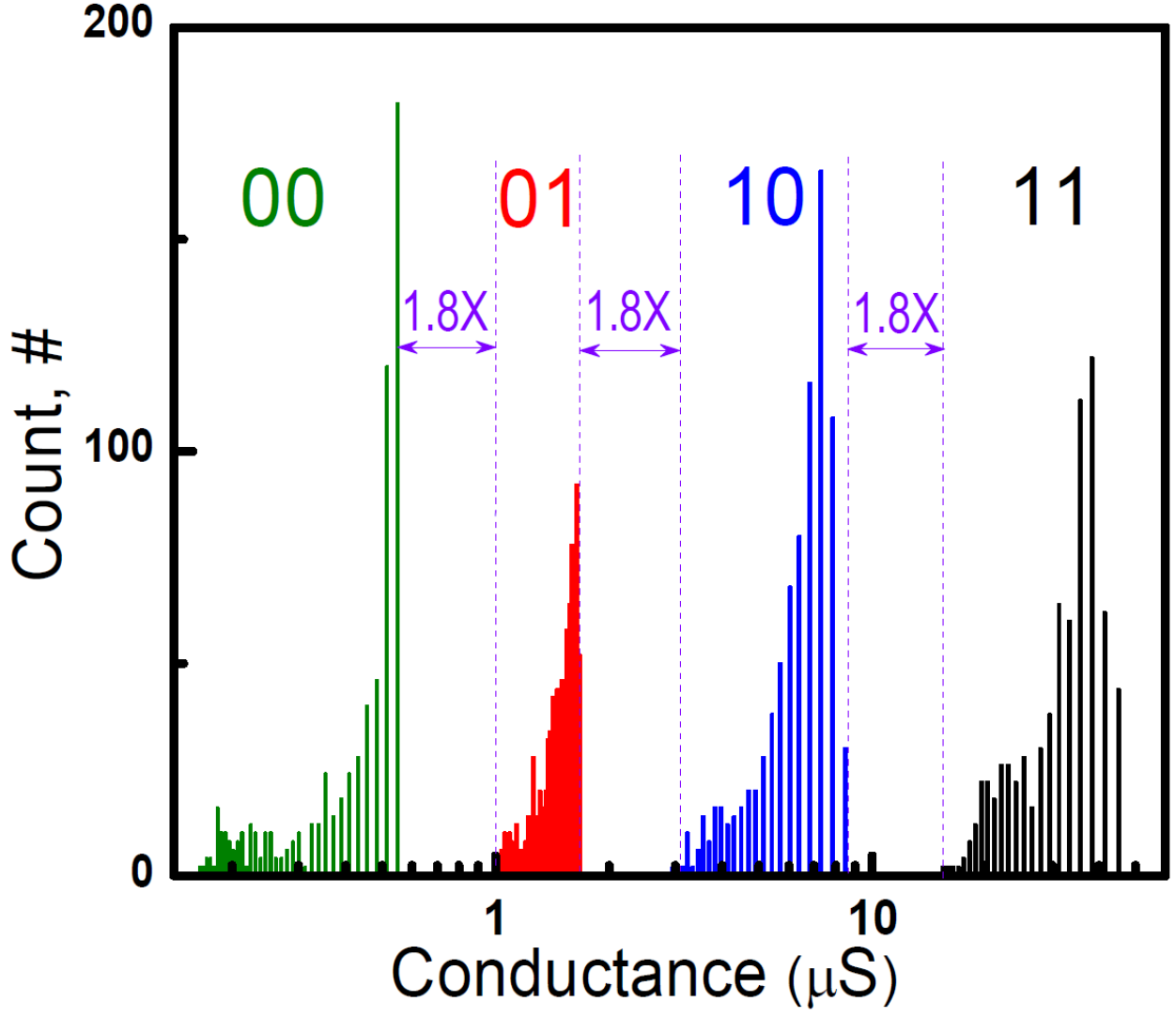
Multi-bit Resistive Switching Memory (RRAM)

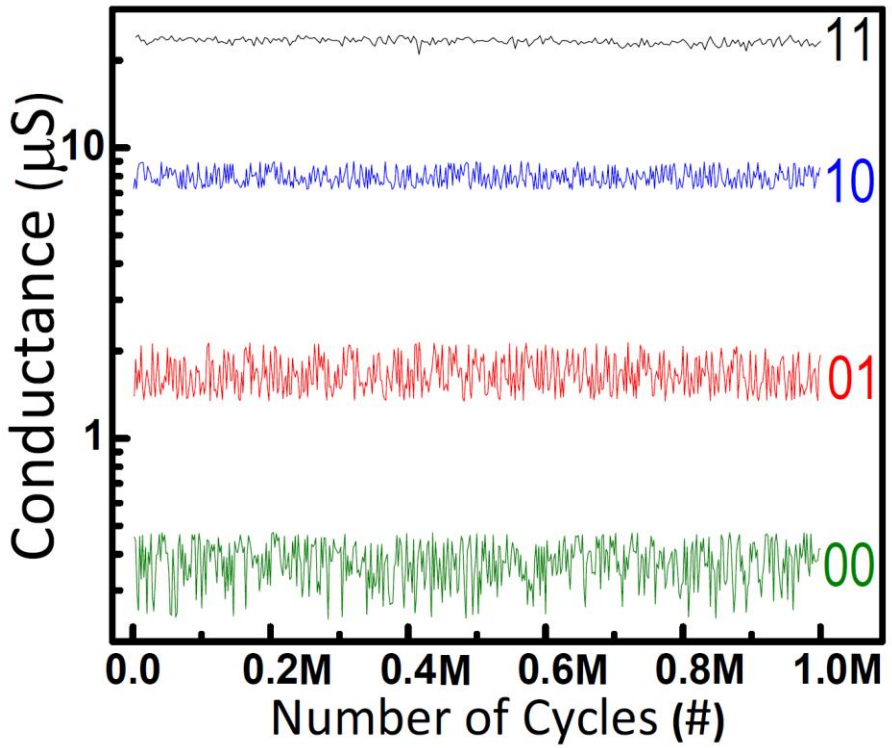


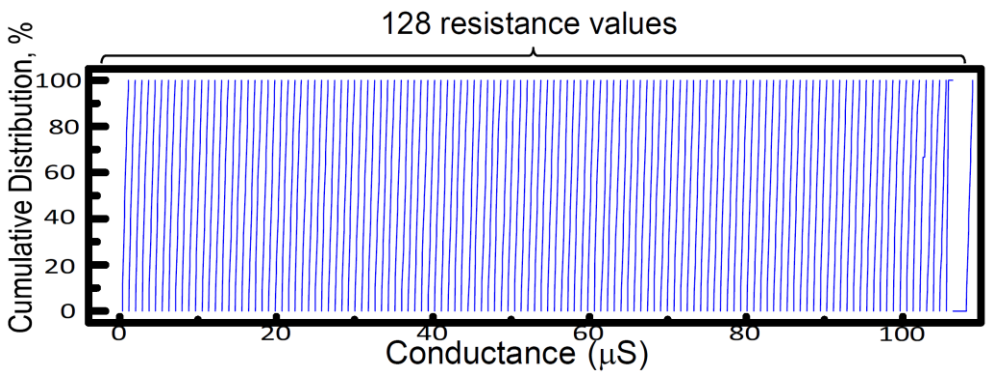


E.R. Hsieh…H.-S. P. Wong, S. Mitra, S. Wong, *IEDM*, paper 35.6 (2019)

Multi-bit Resistive Switching Memory (RRAM)







E.R. Hsieh…H.-S. P. Wong, S. Mitra, S. Wong, *IEDM*, paper 35.6 (2019)

HIGHER MEMORY CAPACITY:

Low Programming Current

< 10 μA programming current to achieve dense layout

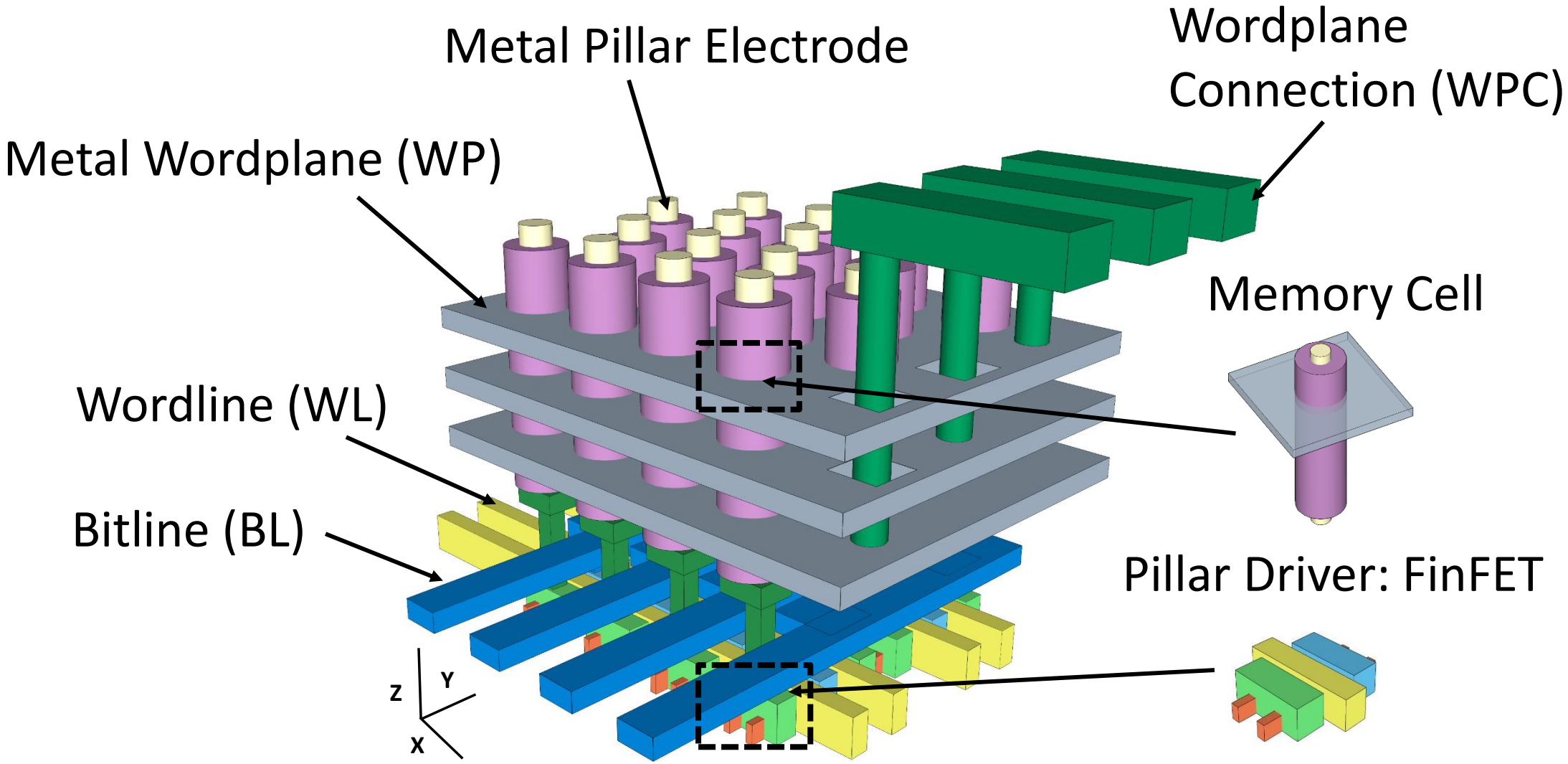
Multi-bit Cell

m-bit per cell = *m* times denser (not incl. peripheral circuitry)

Go 3D!

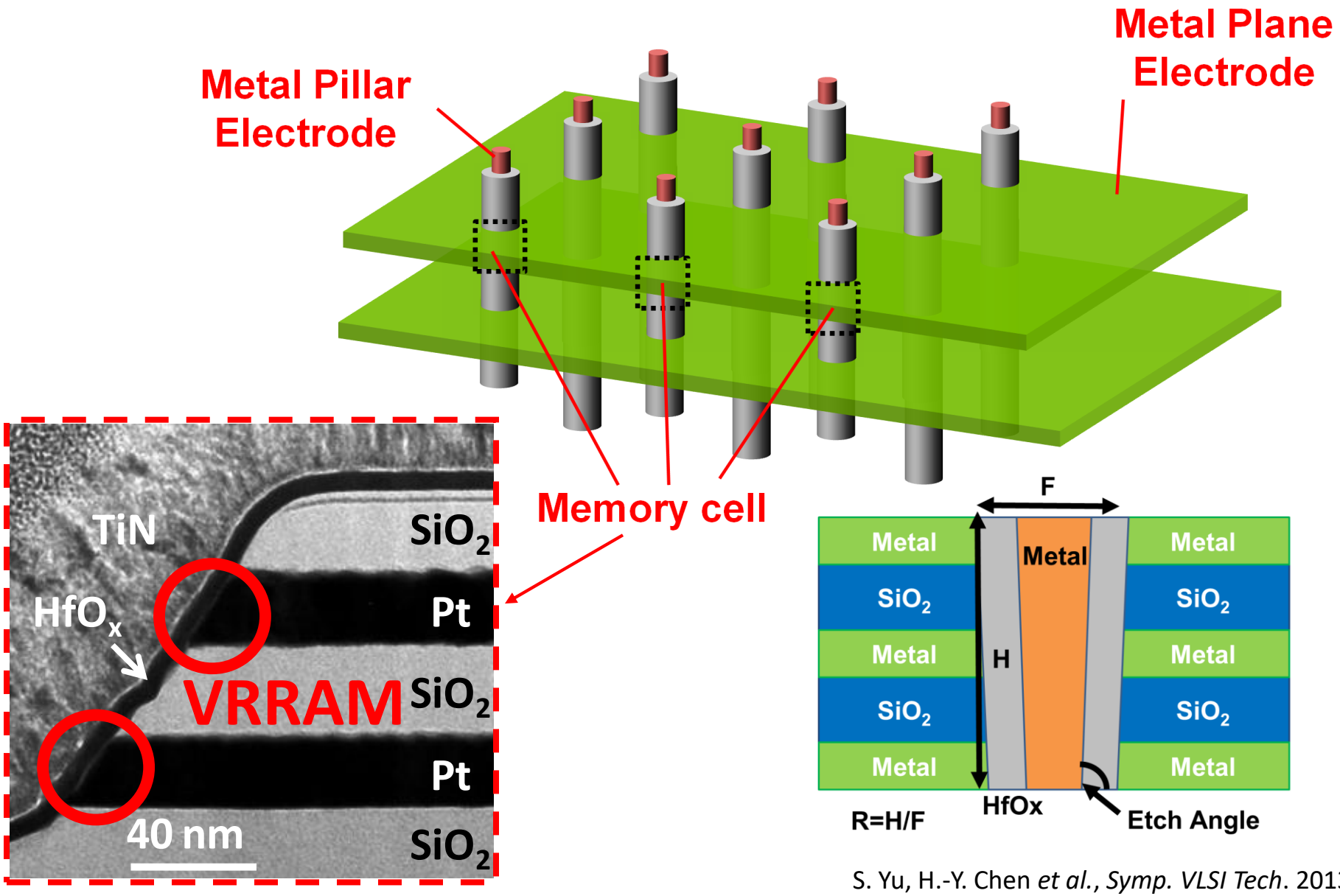
Stack up in the **vertical** direction

Tbit Class 3D Vertical Resistive Switching Memory



Z. Jiang et al., VLSI 2018; S. Qin et al., TED 2019 (Part I); Z. Jiang et al., TED 2019 (Part II)

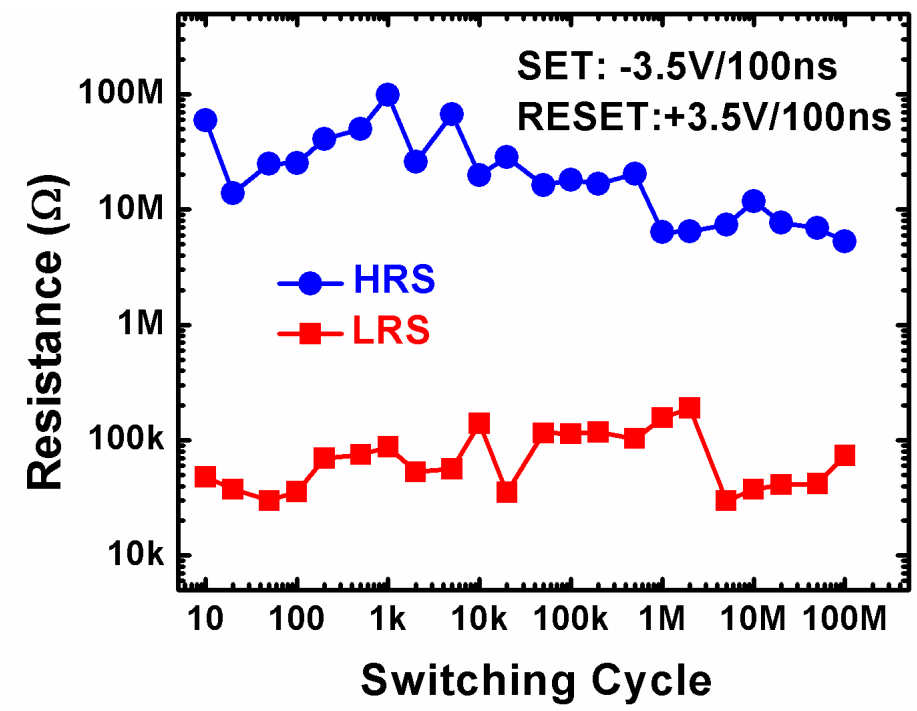
3D RRAM



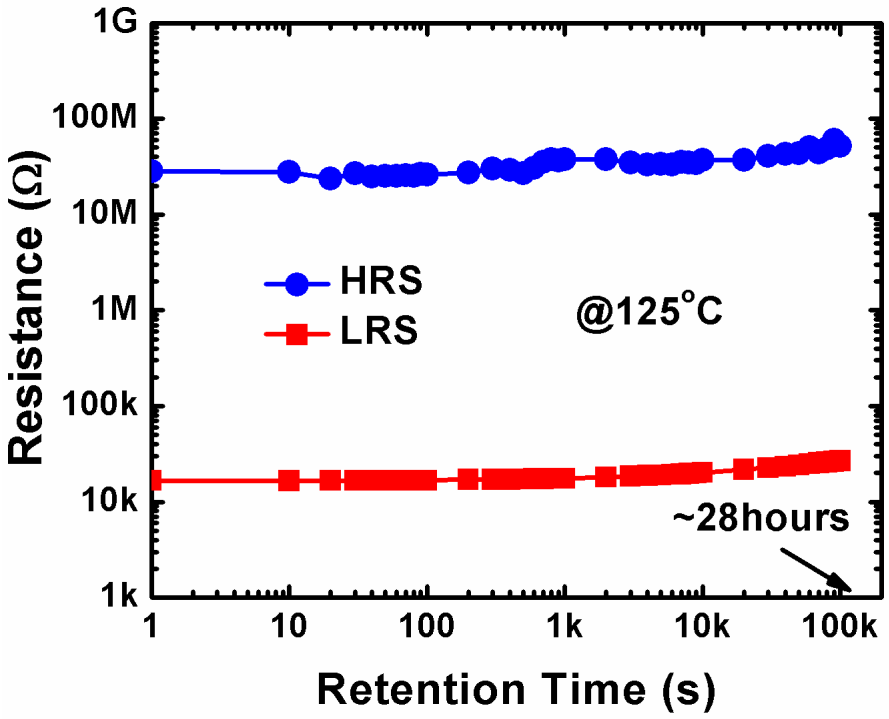
S. Yu, H.-Y. Chen *et al.*, *Symp. VLSI Tech*. 2013

3D RRAM – Realistic Performance

Endurance >10^8 cycles

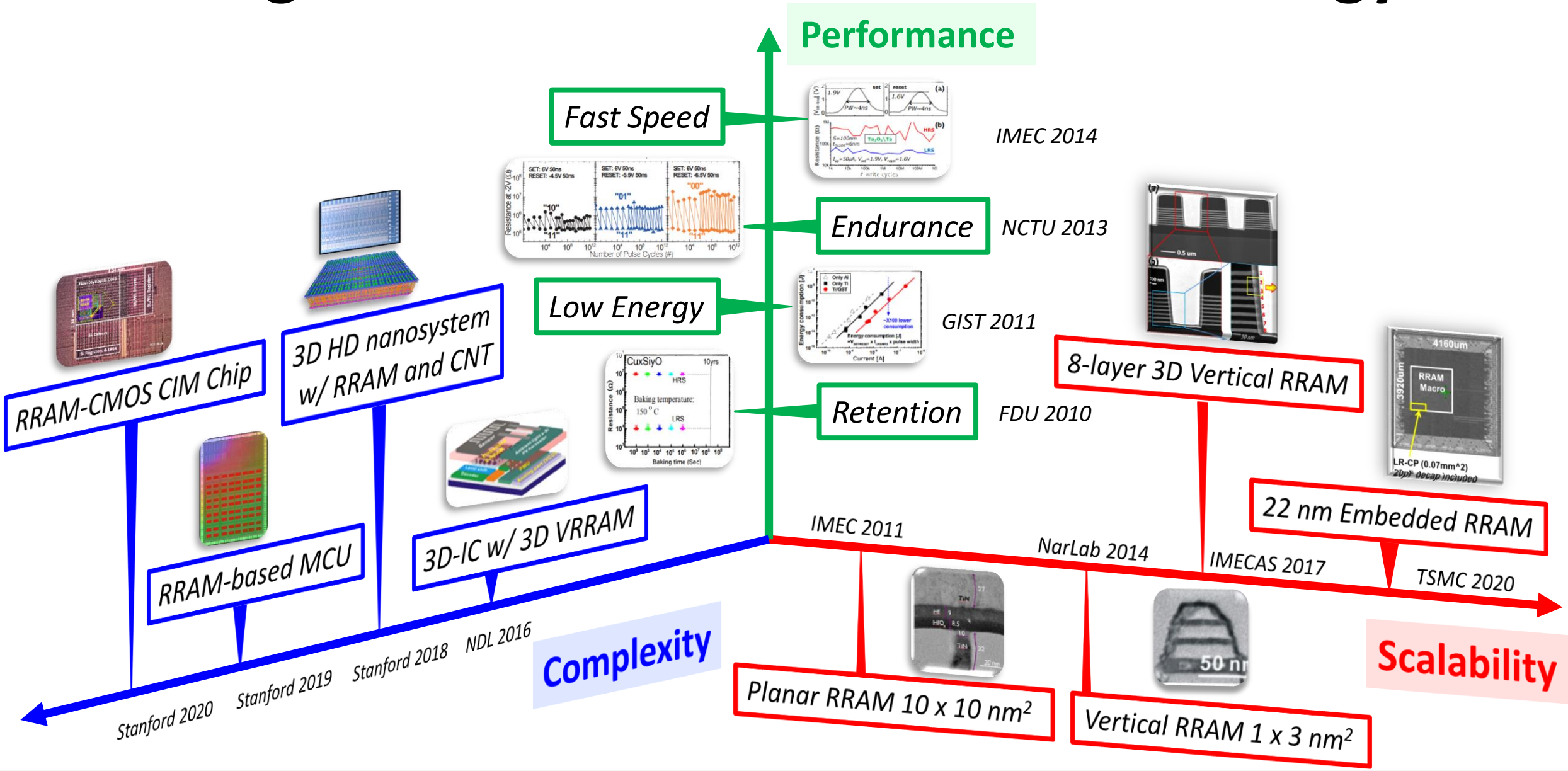


Retention >10^5s @125°C



H.-Y. Chen *et al.*, *IEDM*, 2012

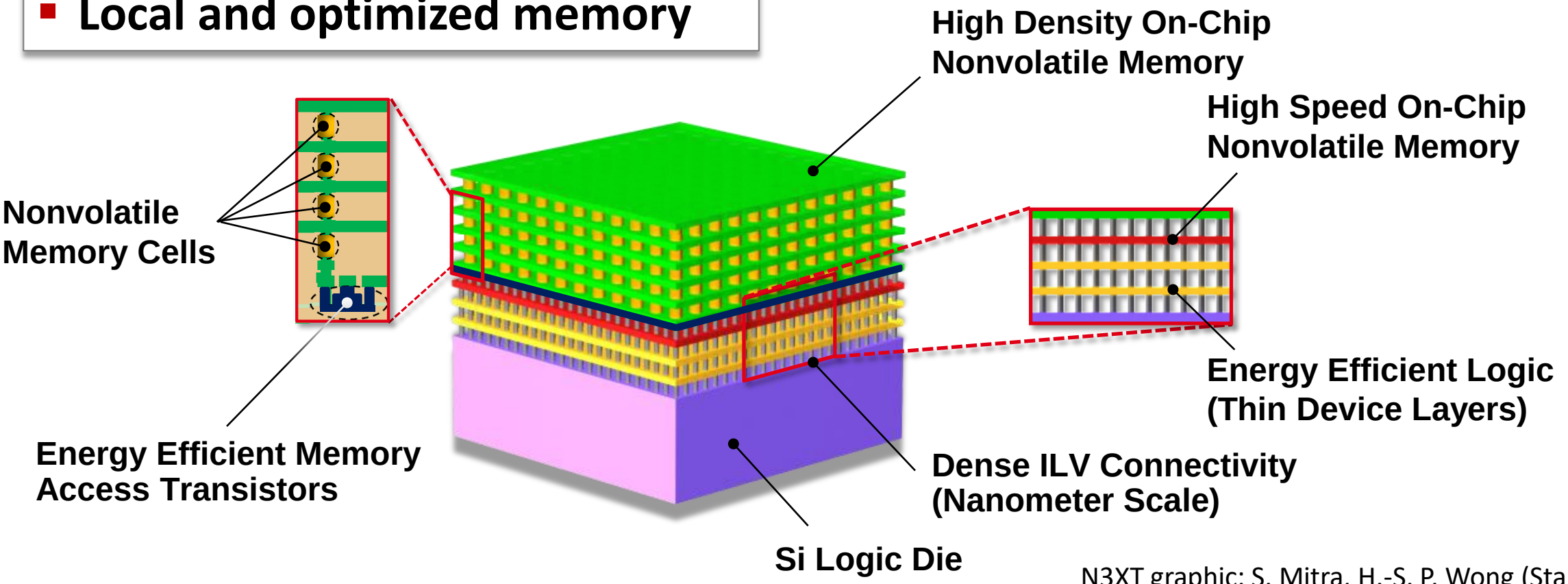
Progress Towards a Practical Technology



THE FUTURE IS SYSTEM INTEGRATION

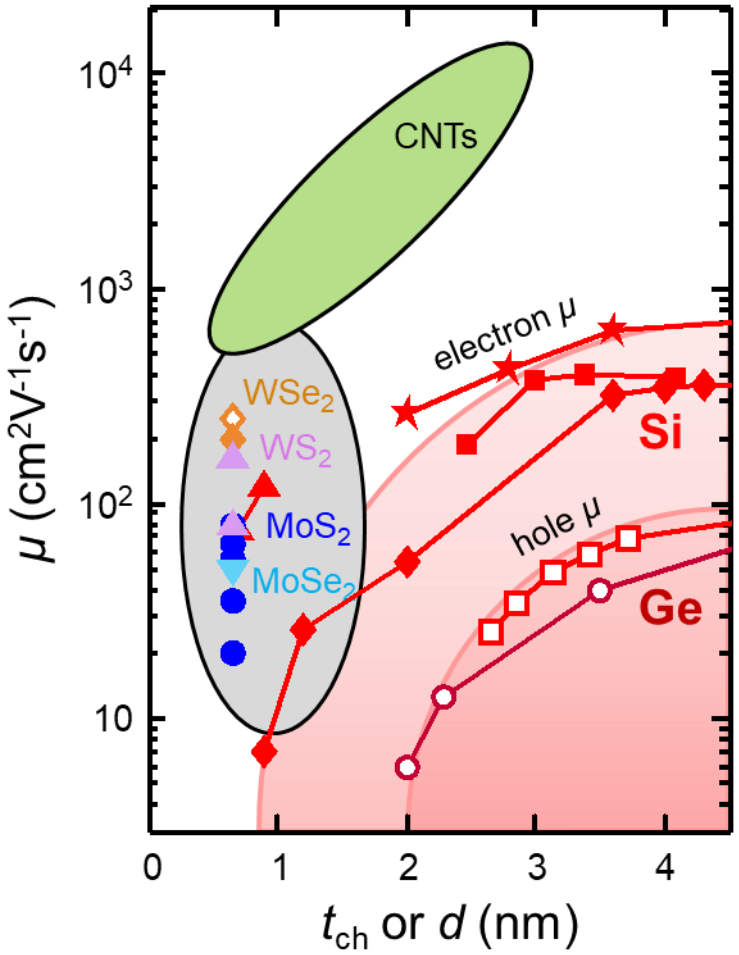
MEMORY INTEGRATED WITH ENERGY-EFFICIENT TRANSISTORS

- **High capacity on-chip memory**
- **Local and optimized memory**

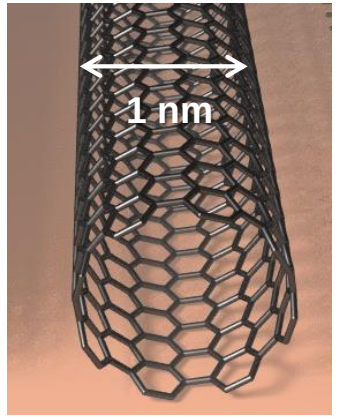


N3XT graphic: S. Mitra, H.-S. P. Wong (Stanford)

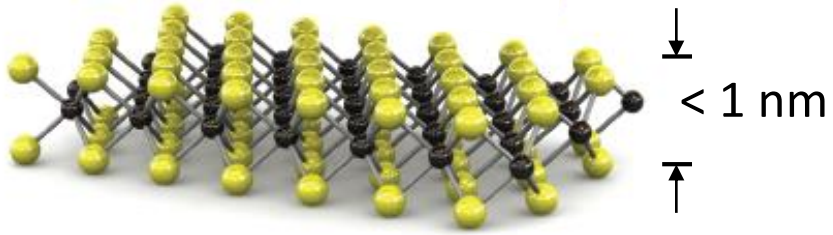
NANOMETER-THIN TRANSISTOR CHANNEL



1D carbon nanotube (CNT)

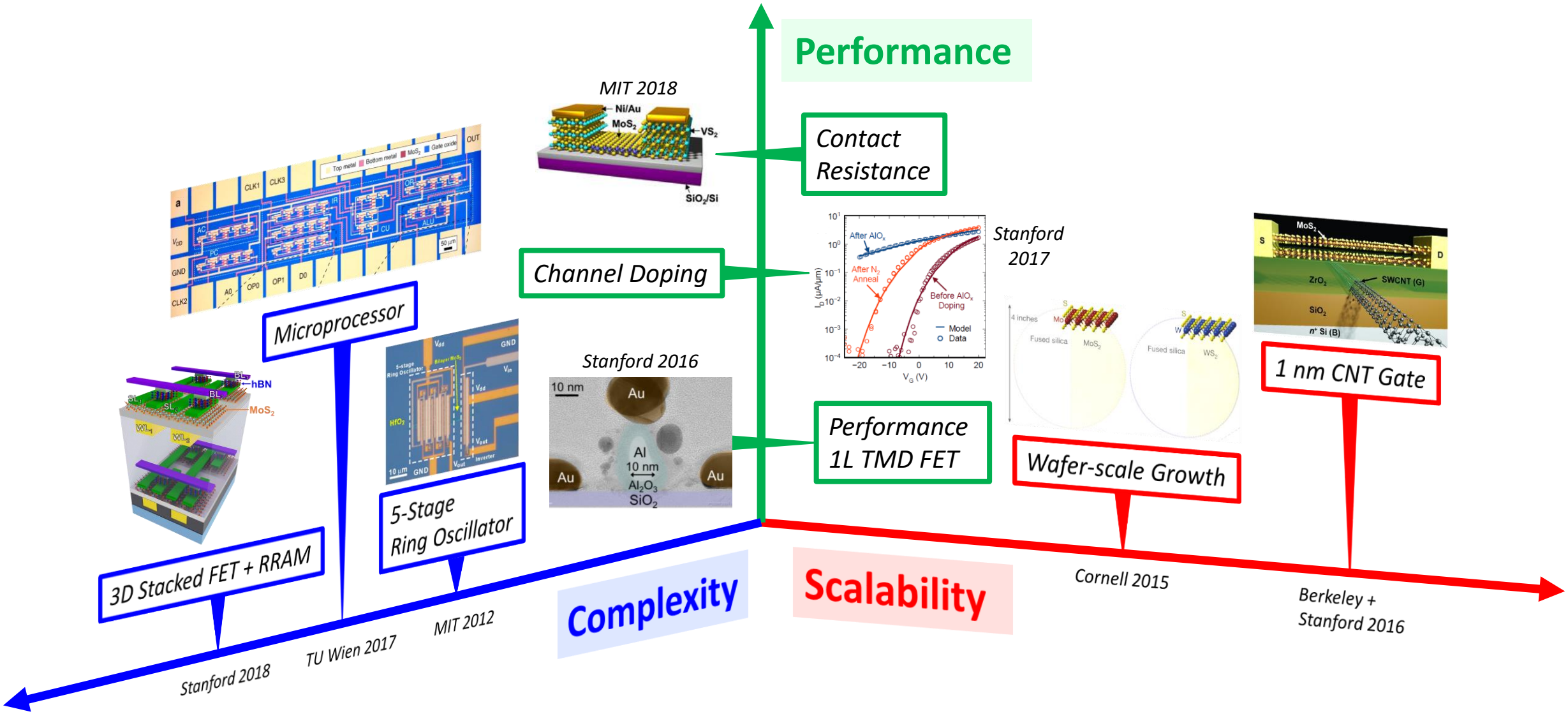


2D Layered Materials
e.g. Transition Metal Dichalcogenides
(TMD: MoS_2, WS_2, WSe_2, WTe_2, …), BP, aGNR



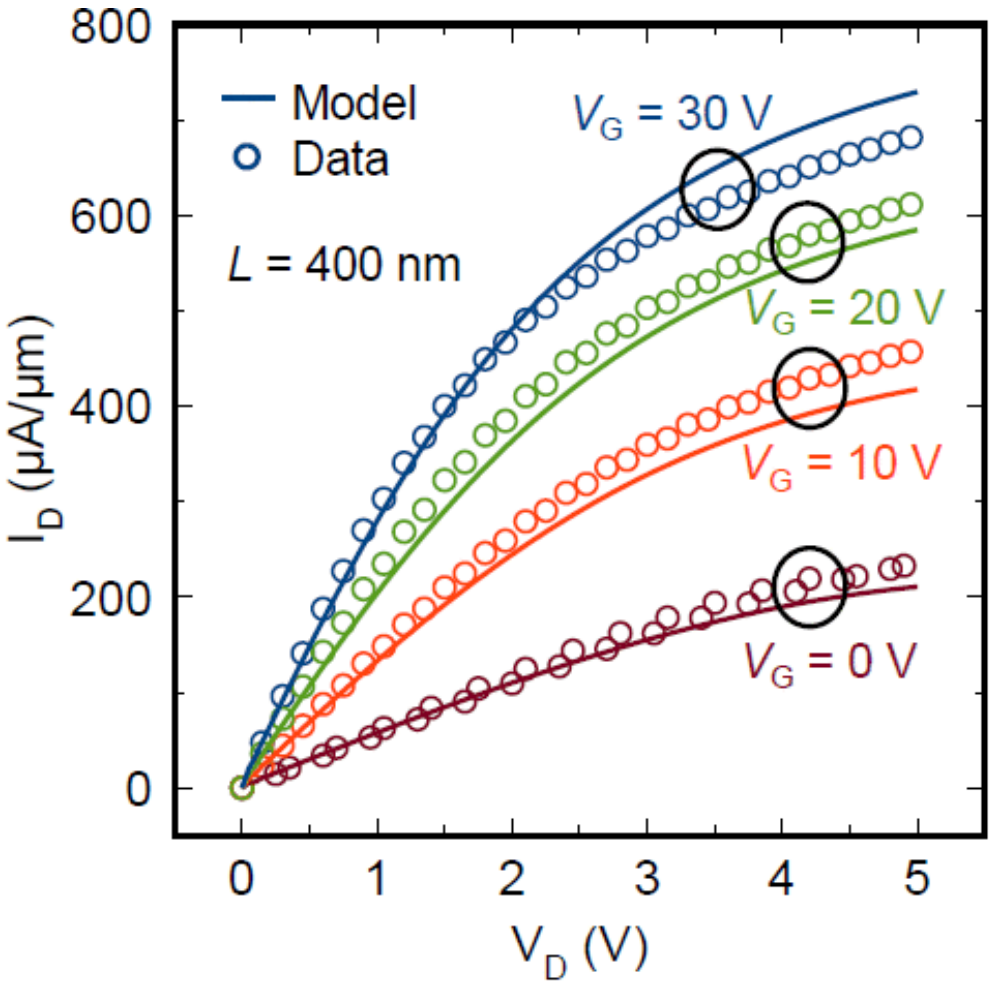
sources: K. Uchida, A. Kis, IBM, E. Pop (C. English, Nano Lett '16)

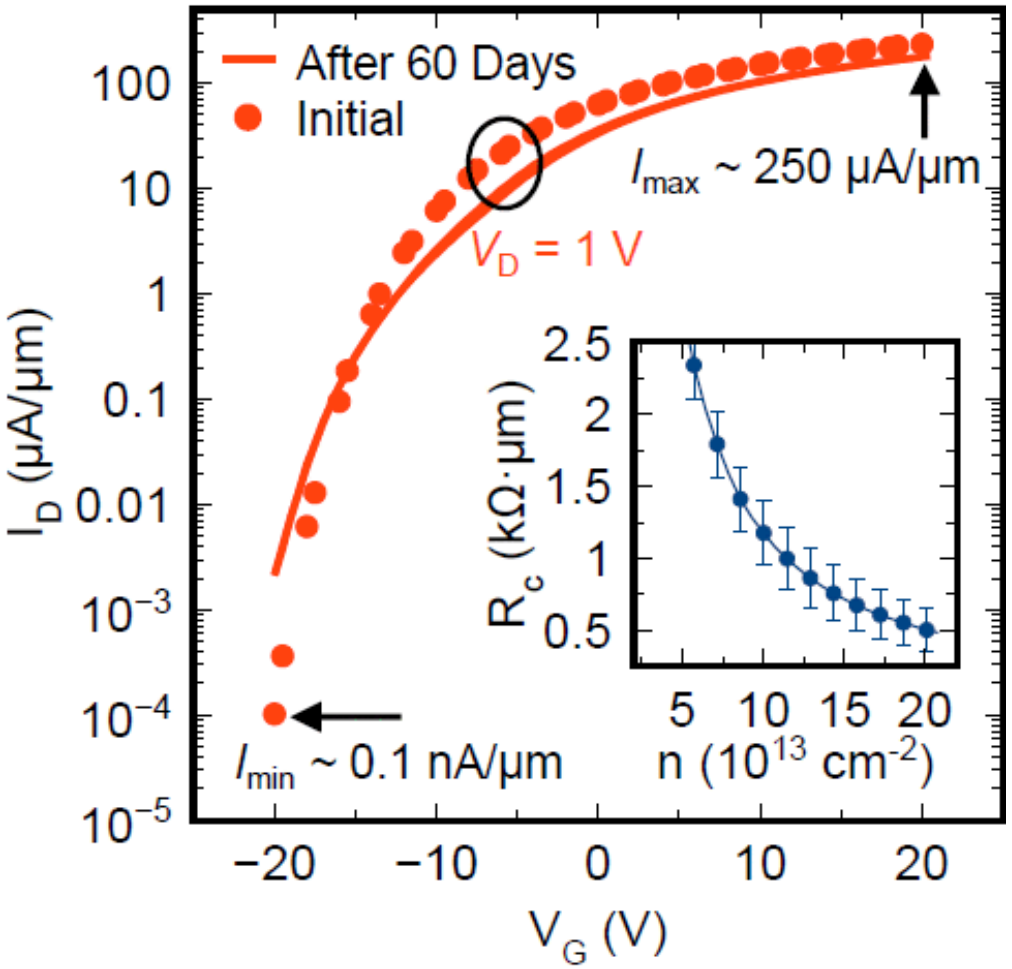
Progress Towards a Practical Technology



1L MoS_2 TRANSISTOR

RECORD: I_{ON} = 700 μA/μm, R_C = 480 Ω·μm

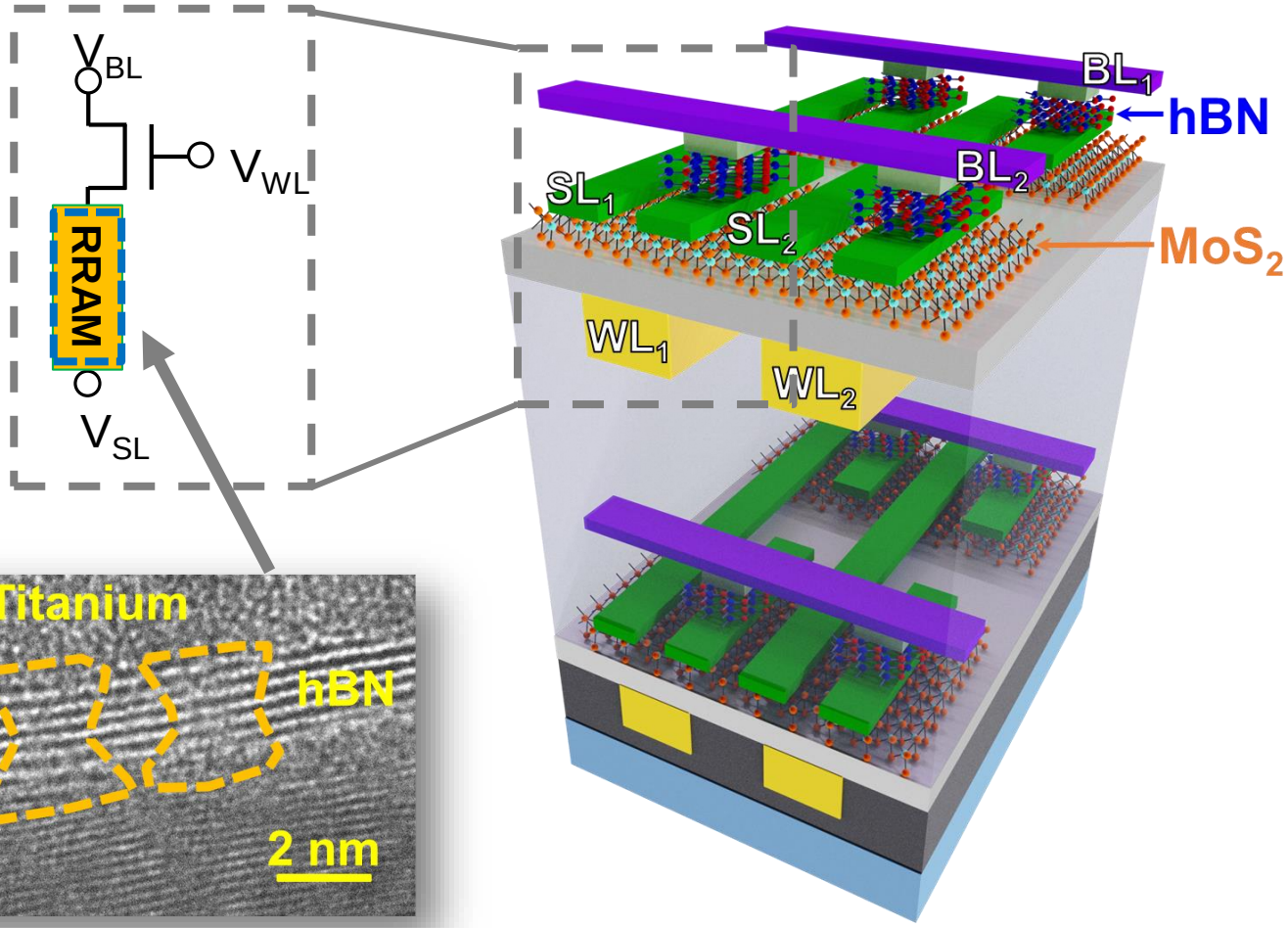


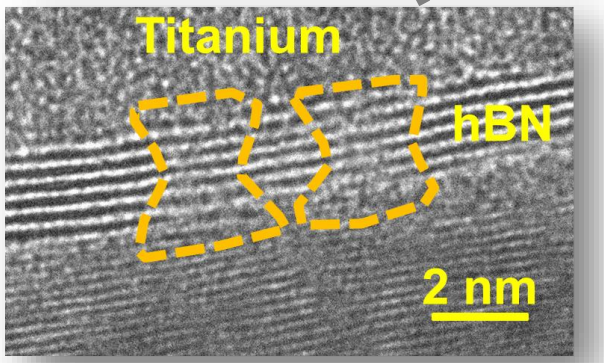


McClellan et al. (Stanford), *DRC 2017*, pp. 1-2

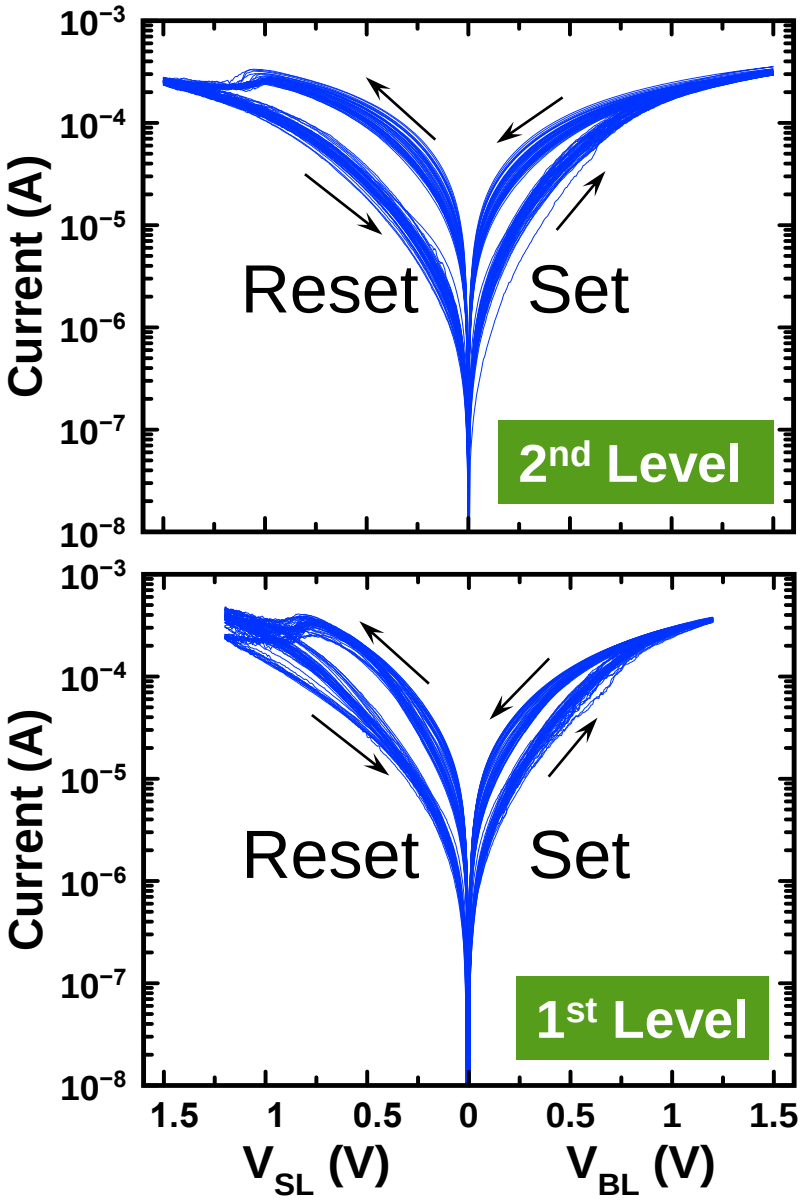
3D INTEGRATION:

(MoS_2 TRANSISTOR + RRAM) x **2 LAYERS**





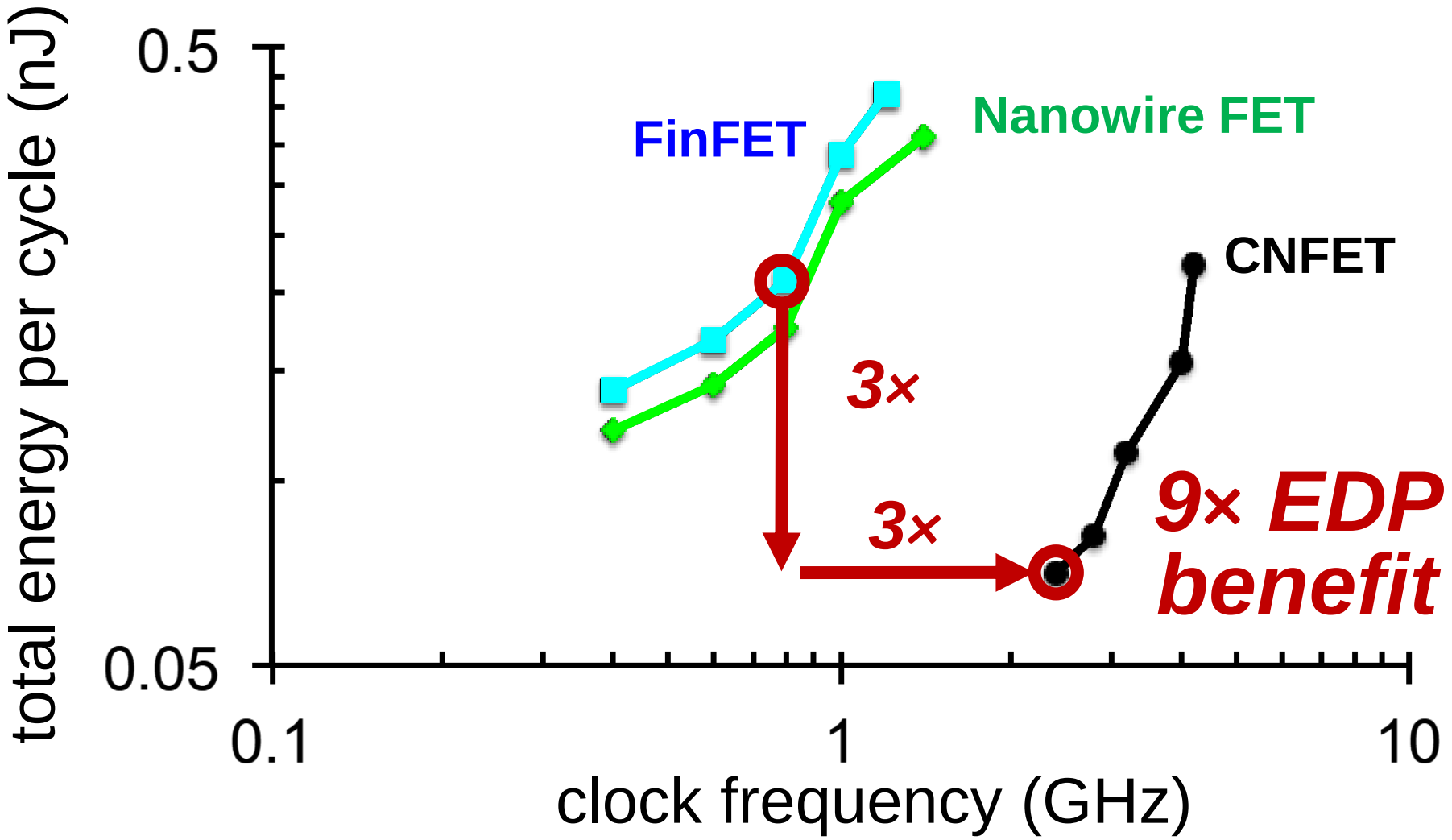
Y. Shi, … E. Pop, H.-S. P. Wong, M. Lanza, *IEDM*, paper 5.4, 2017

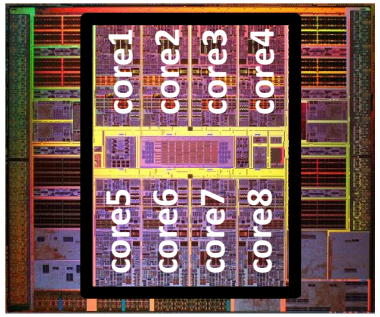


C.-H. Wang… M. Lanza, E. Pop, H.-S. P. Wong (Stanford, Soochow U), *IEDM 2018*, paper 22.5

CARBON NANOTUBE TRANSISTOR

9X BETTER THAN SILICON TRANSISTOR

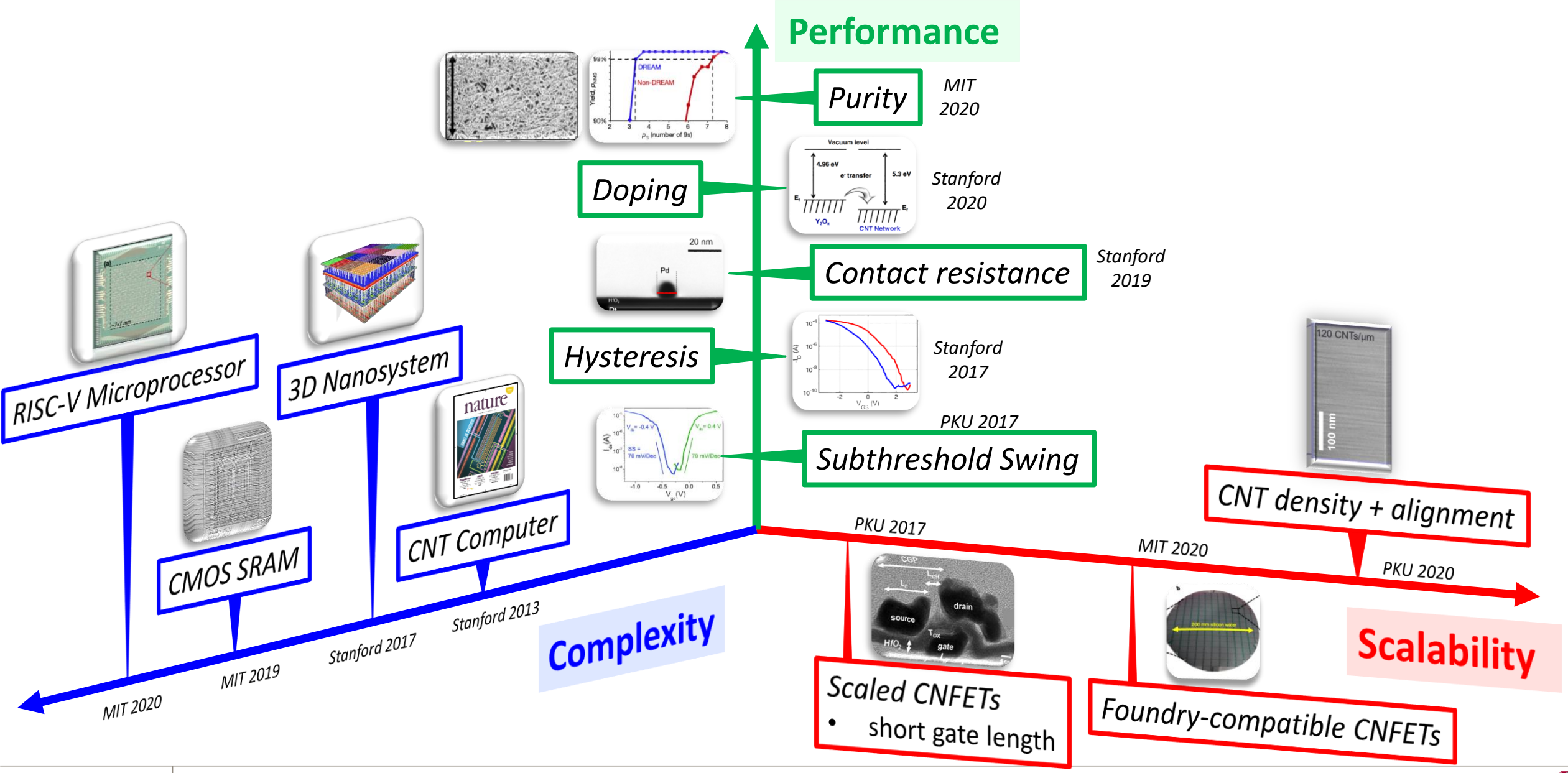




- OpenSPARC T2 processor core
- full physical design
- 32 million FETs

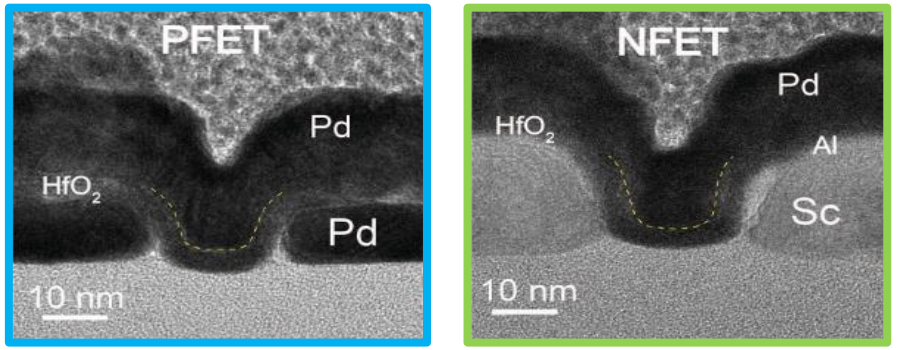
G. Hills,… H.-S. P. Wong, S. Mitra (Stanford, IMEC, TSMC, NUS, MIT) , *IEEE T-NANO*, p. 1259, 2018

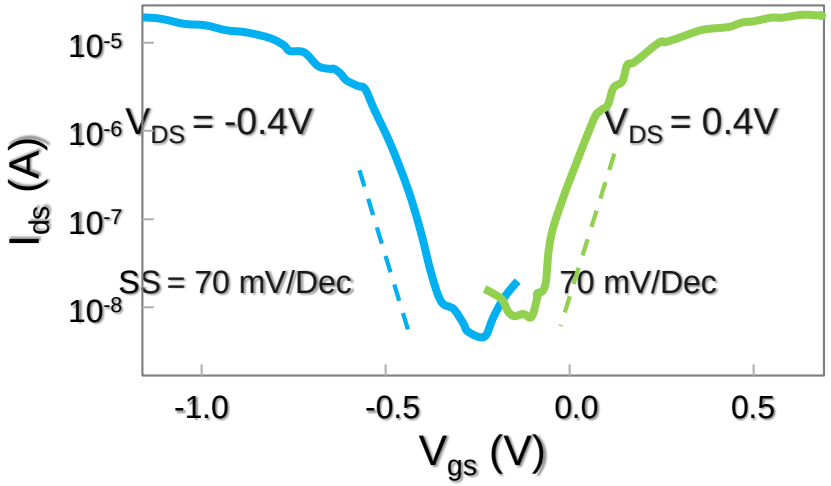
Progress Towards a Practical Technology



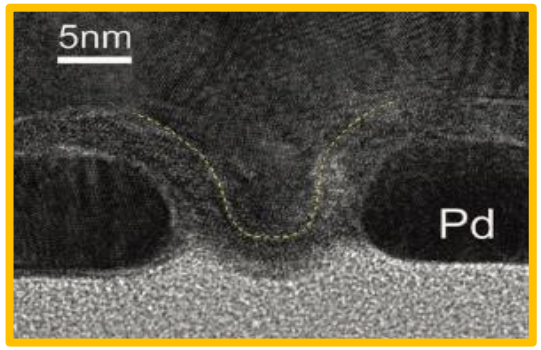
SHORT-CHANNEL
CARBON NANOTUBE TRANSISTORS

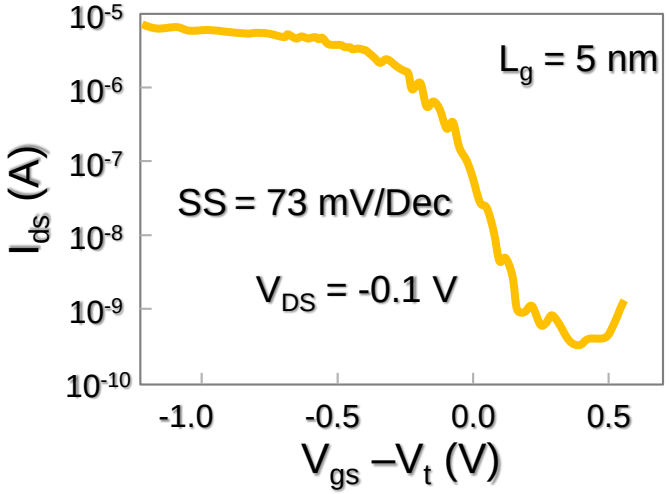
10 nm Gate Length





5 nm Gate Length

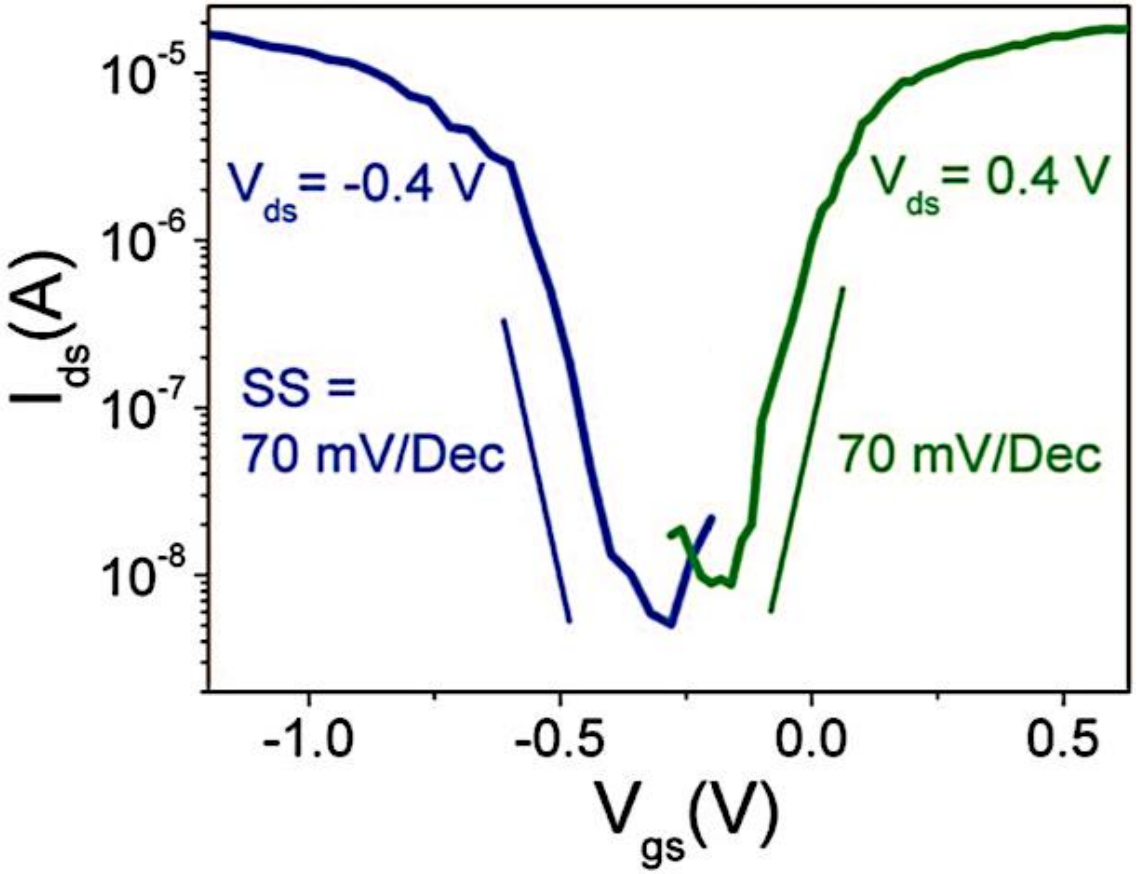




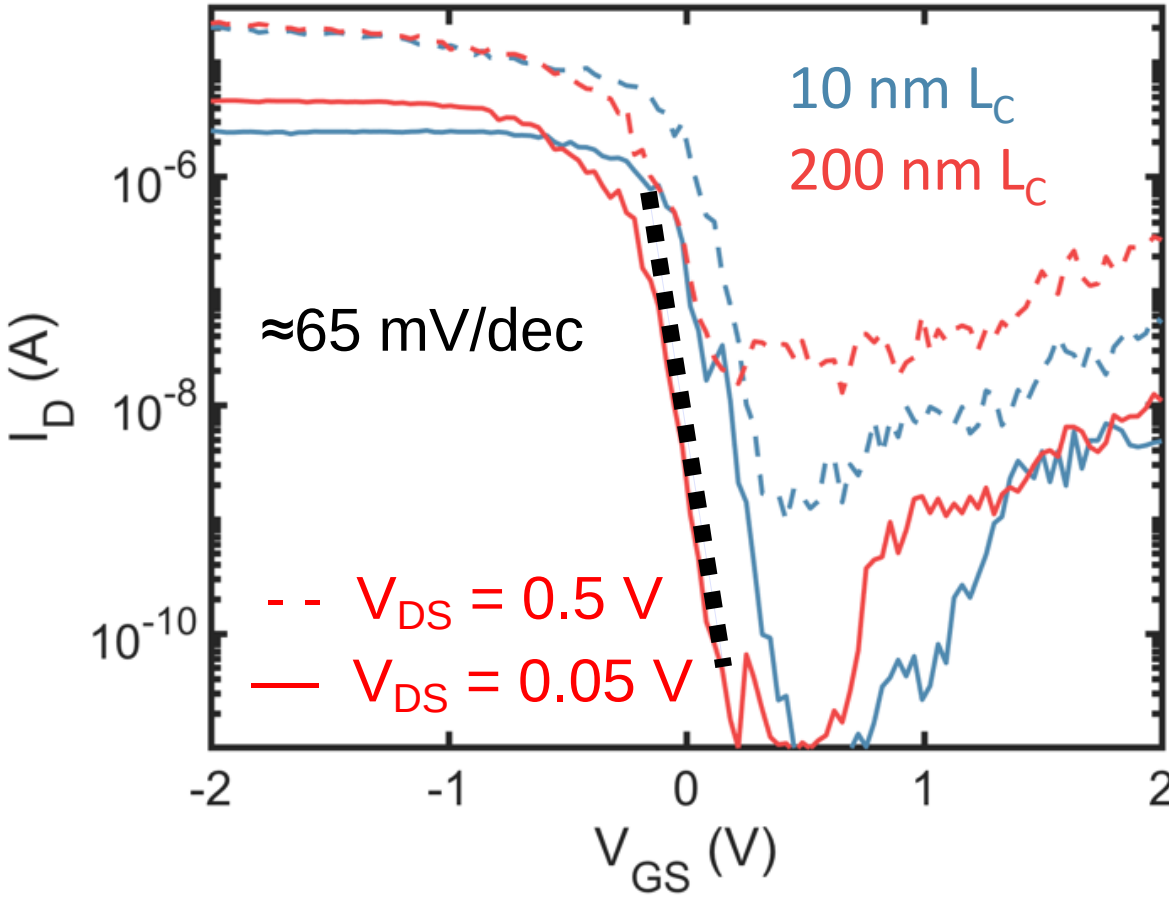
C. Qui,…L.-M. Peng (PKU), *Science*, 2017

LOW SUBTHRESHOLD SWING for Low Power

10 nm gate length



≈10 nm contact length

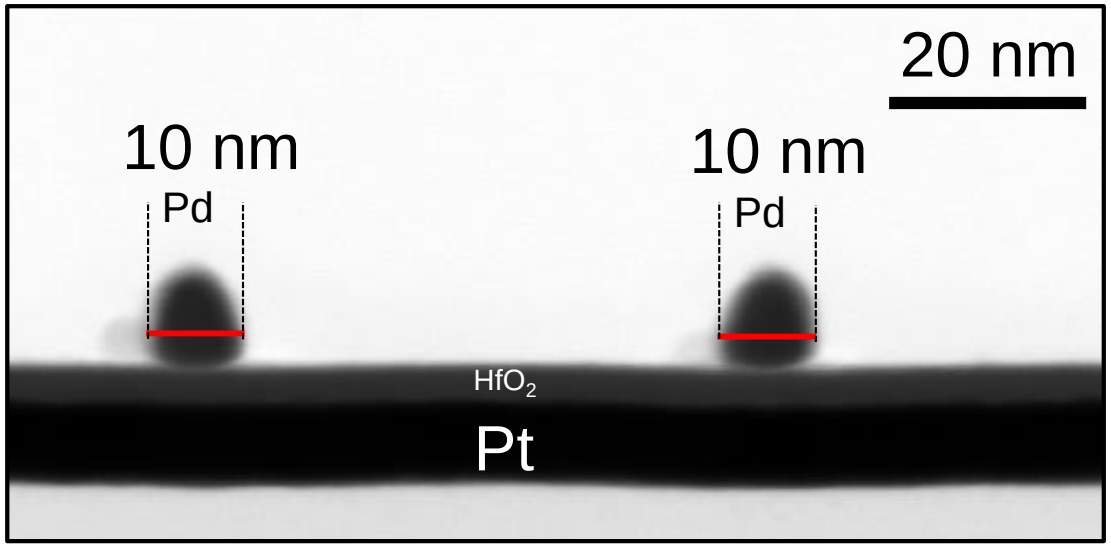


C. Qiu,…L-M. Peng (PKU), *Science,* 2017

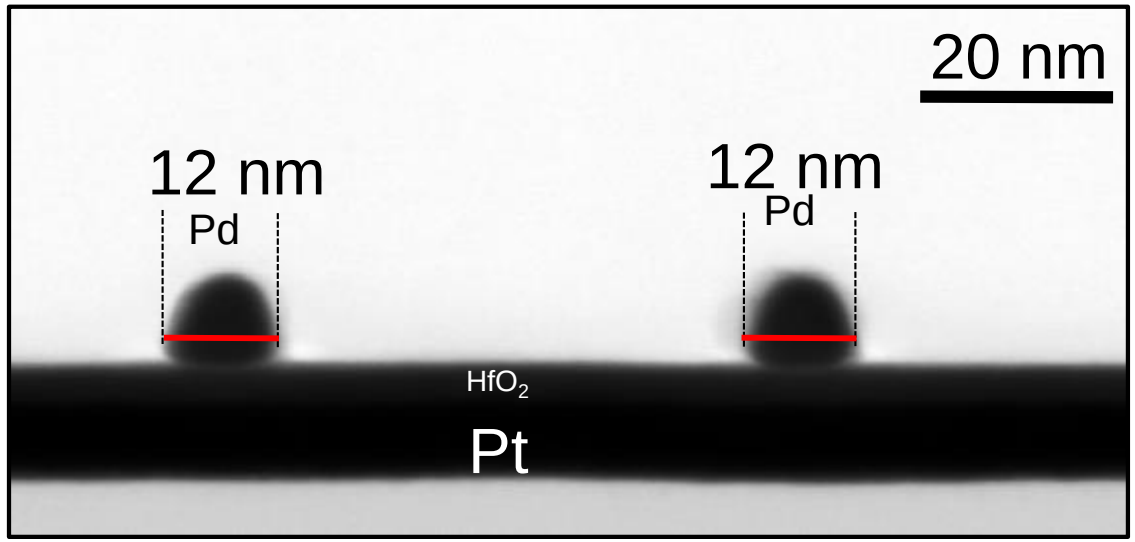
G. Pitner (Stanford), *PhD Thesis*, 2018

10-NM CONTACT TO CARBON NANOTUBE

Measured R_C = 7.6 kΩ



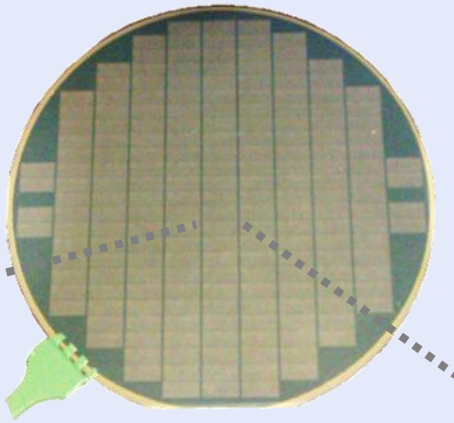
Measured R_C = 6.5 kΩ

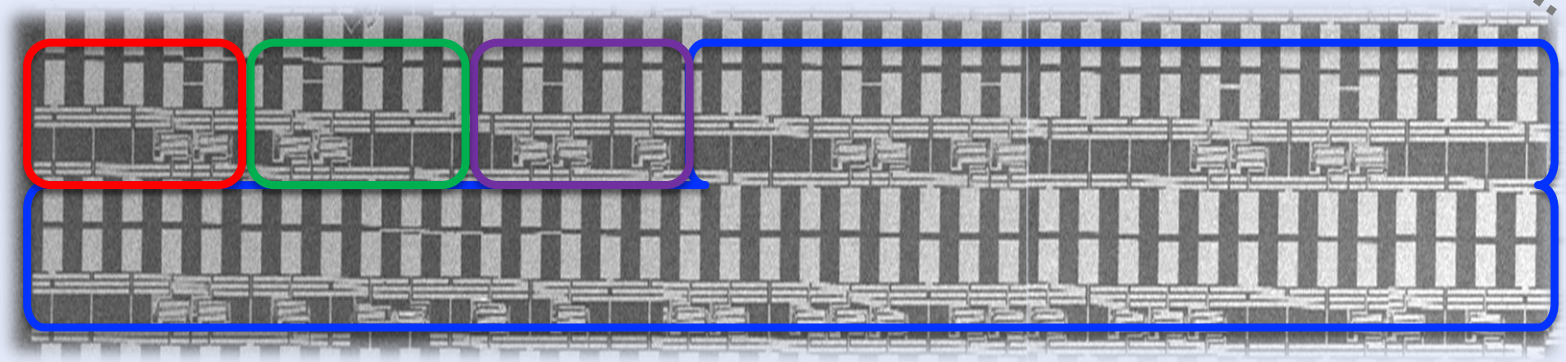


At metal-CNT interface at CNT, the contact dimension is smaller

G. Pitner,… H.-S. P. Wong (Stanford), *Nano Lett.*, 2019

NANOSYSTEM: CARBON NANOTUBE COMPUTER

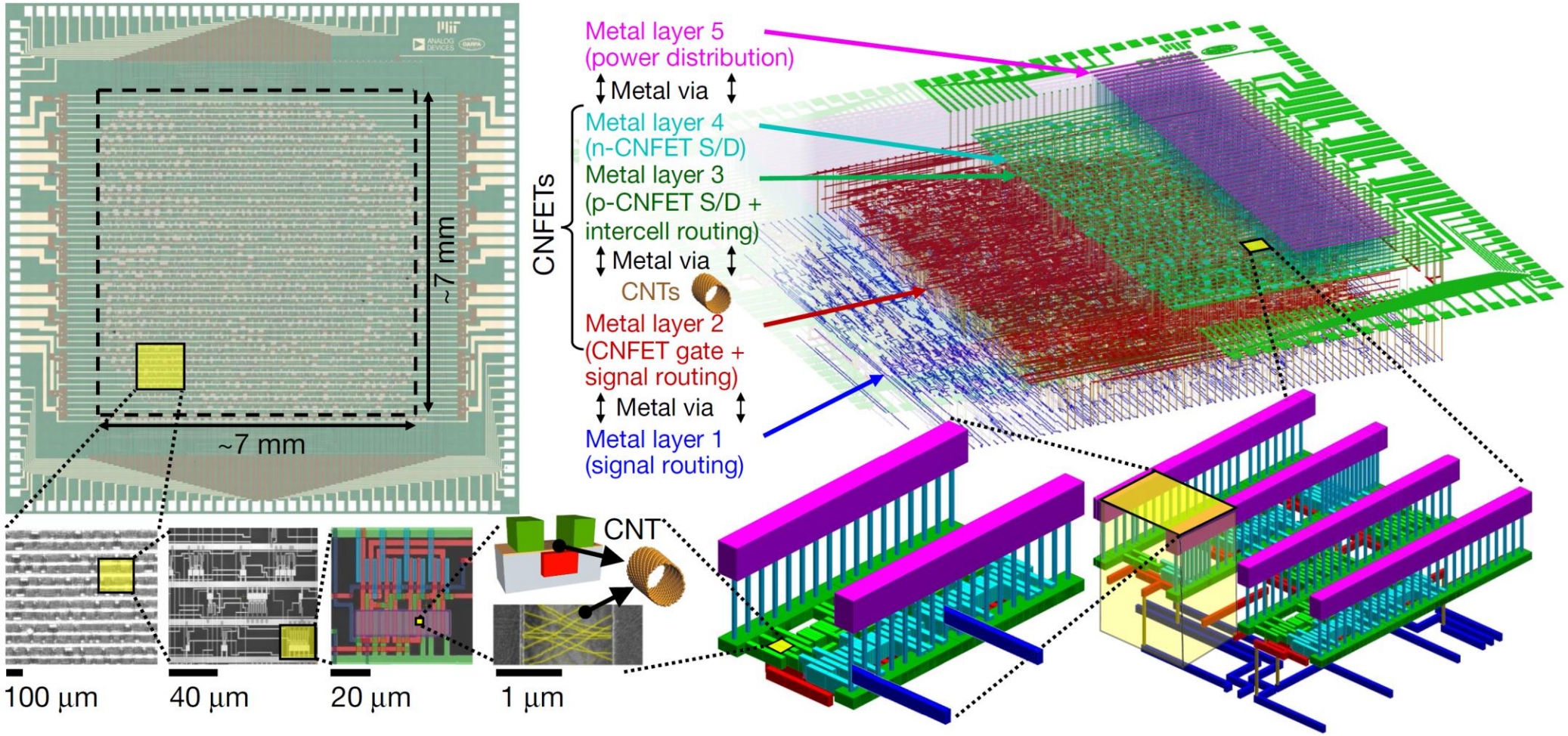




instruction fetch **data fetch** **arithmetic block** **write-back**

M. Shulaker,…H.-S. P. Wong, S. Mitra (Stanford), *Nature*, 2013

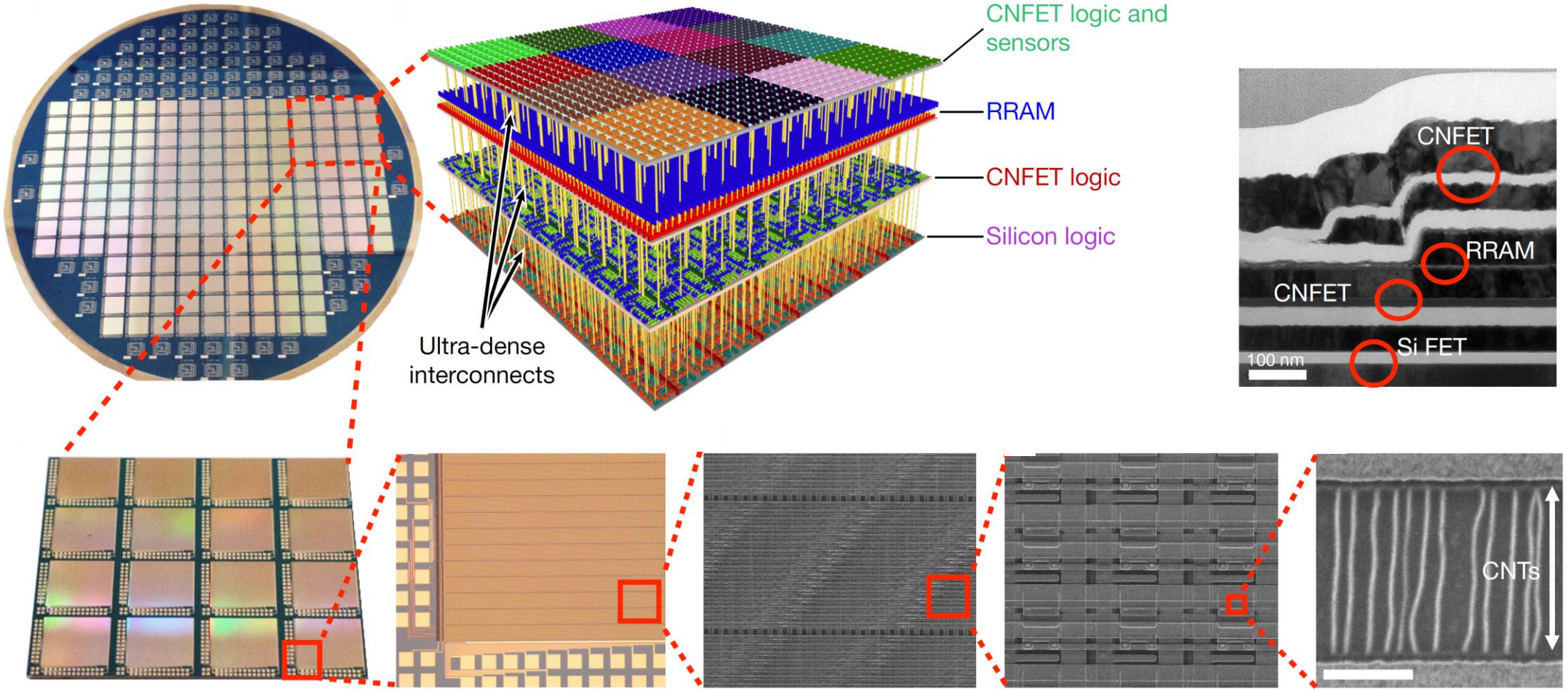
CARBON NANOTUBE RISC-V PROCESSOR



G. Hills… M. Shulaker (MIT), *Nature*, 2019

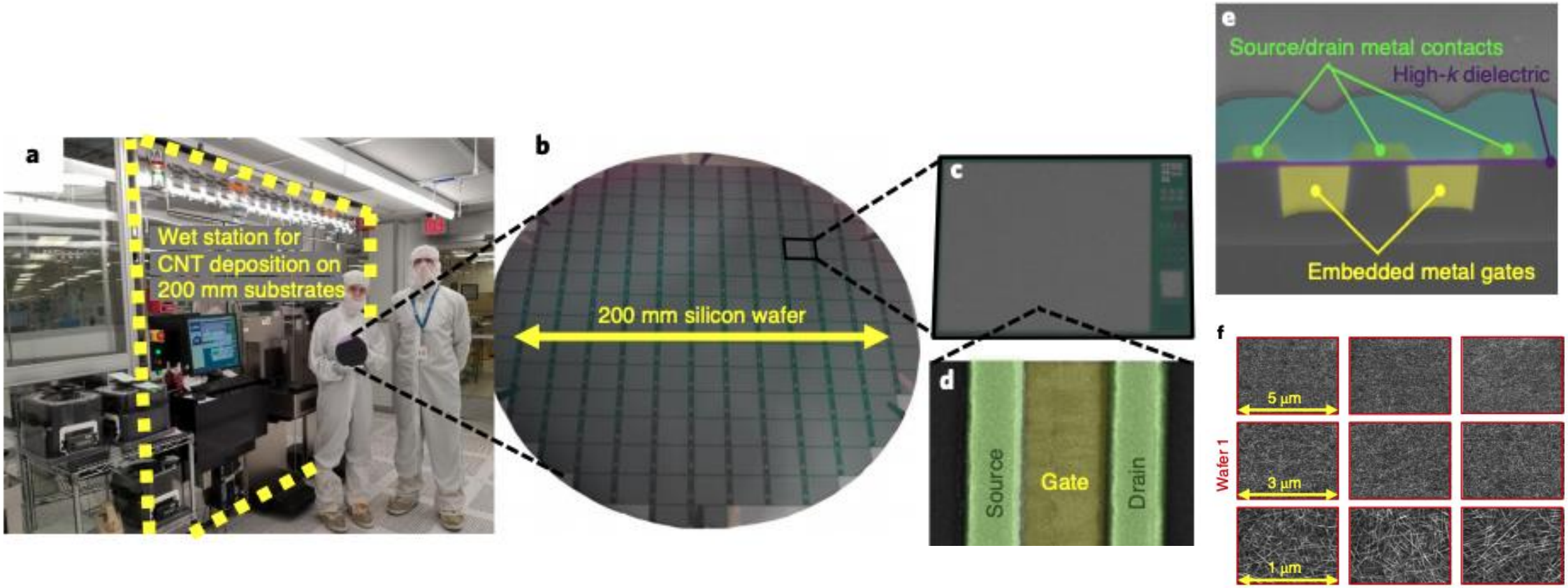
N3XT NANOSYSTEM

> 2 MILLION CNFETS, 1 MBIT RRAM



M. Shulaker,…H.-S. P. Wong, S. Mitra (Stanford), *Nature*, 2017

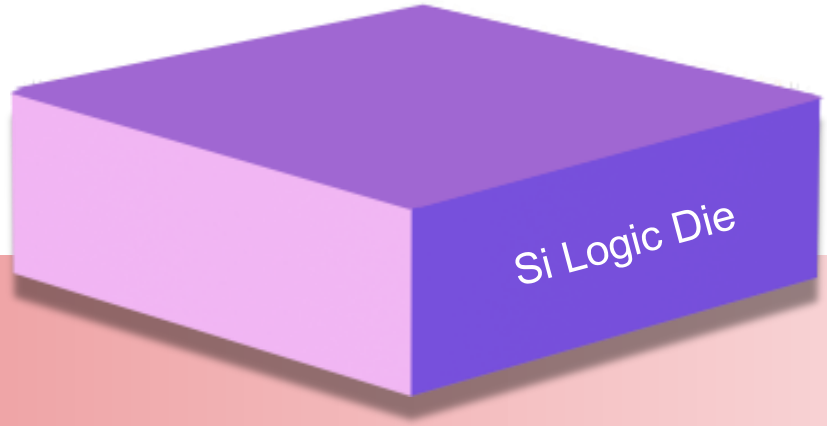
TRANSLATION TO CHIP FOUNDRY



M. Bishop,…M. M. Shulaker. (MIT), *Nat. Electron.*, 2020

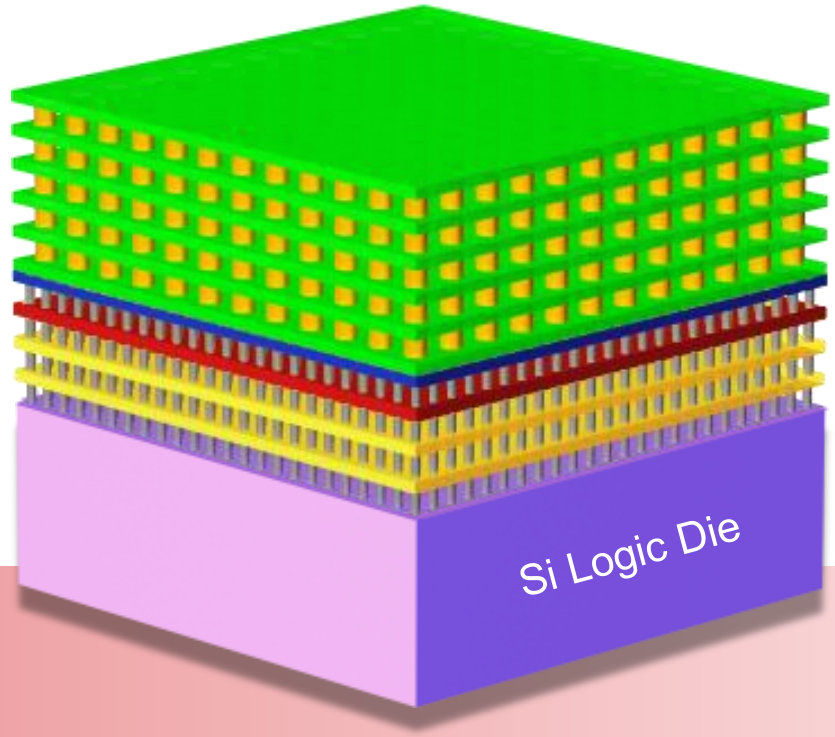
MEMORY INTEGRATION
ON LOGIC PLATFORM

✗ Better transistor alone

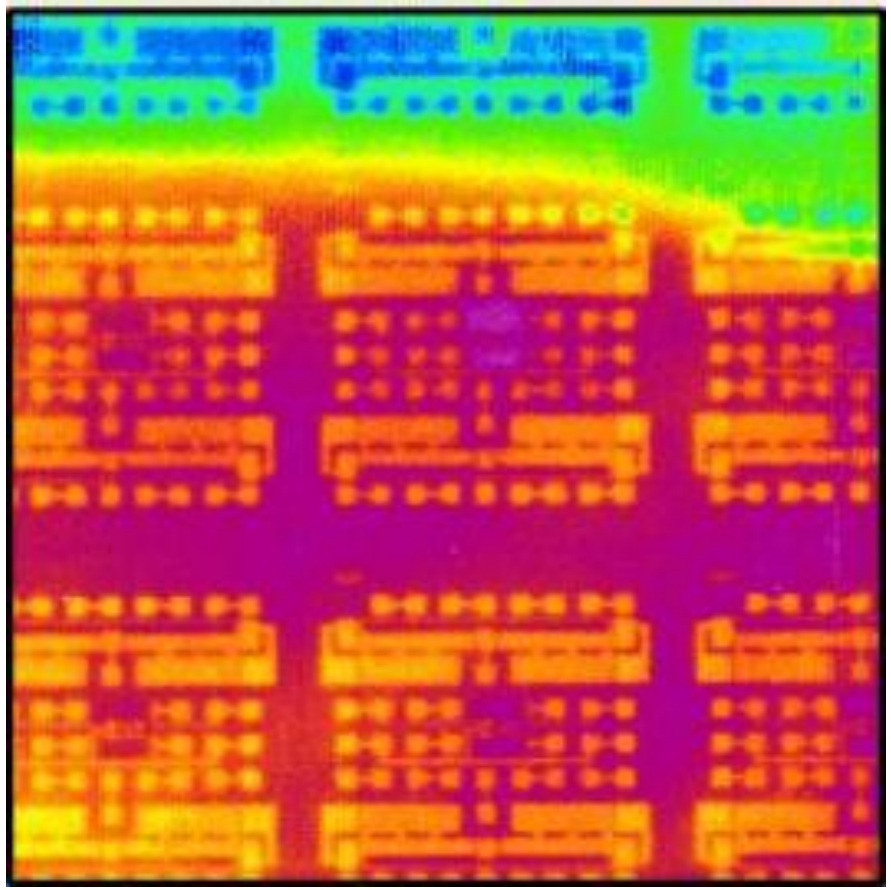


MEMORY INTEGRATION
ON LOGIC PLATFORM

✓ Transistors integrated with memory in **3D**



THERMAL MANAGEMENT



Hot spot image: Prof. K. Goodson (Stanford)

N3XT NanoSystem

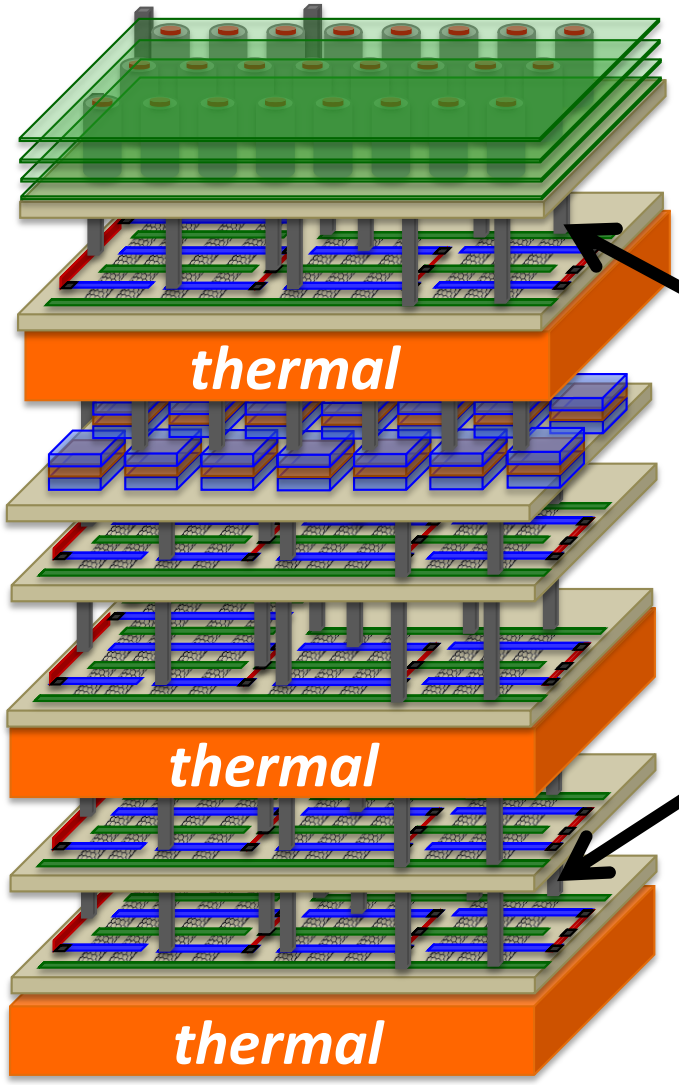
3D Resistive RAM
Massive storage

1D CNFET, 2D FET
Compute, RAM access

MRAM
Quick access

1D CNFET, 2D FET
Compute, RAM access

1D CNFET, 2D FET
Compute, Power, Clock



Not TSV

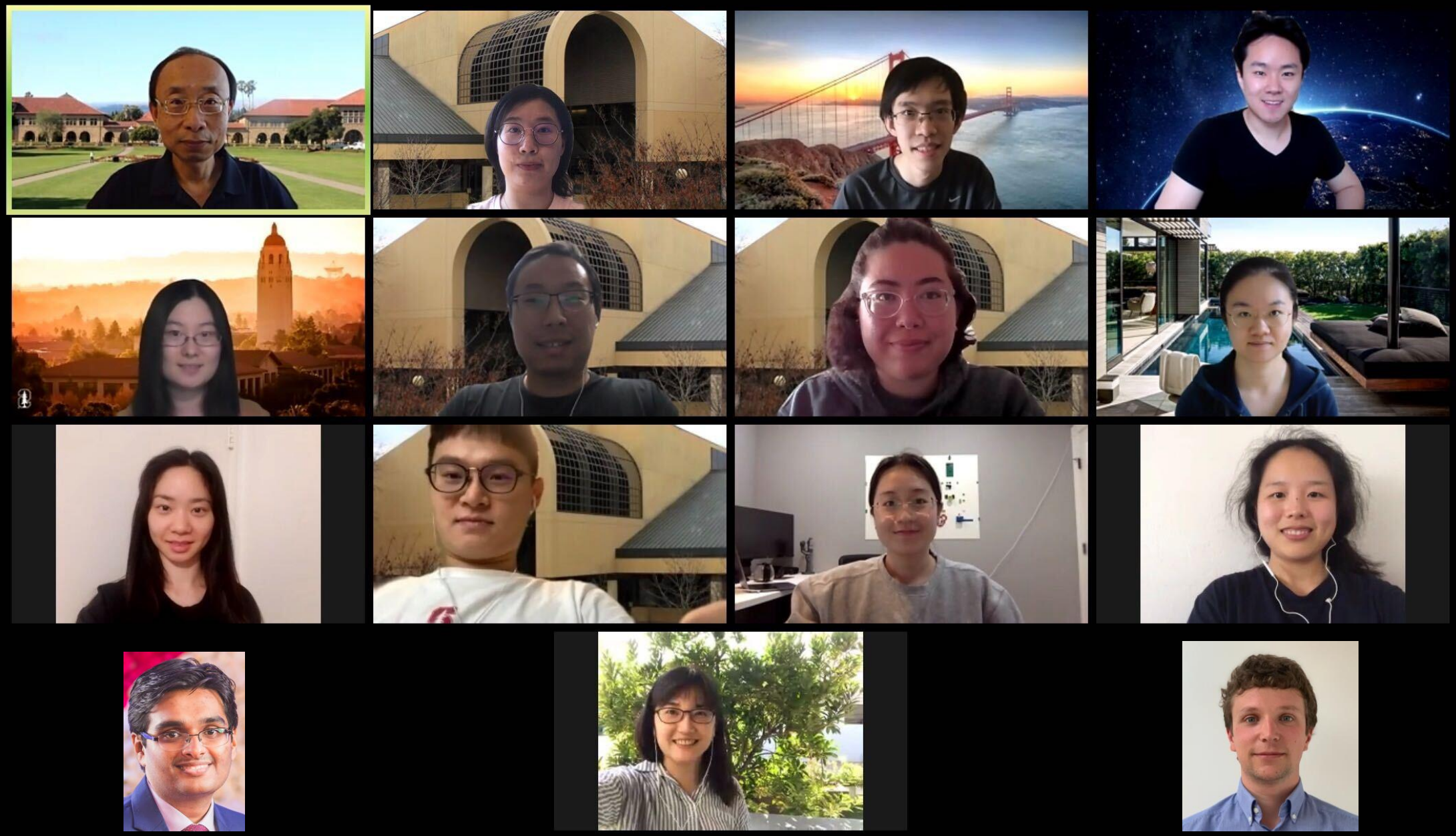
Ultra-dense,
fine-grained vias

Silicon compatible

M. Aly et al., *IEEE Computer*, 2015

Photo by Kasuma from Pexels

Students and Post-Docs @ Stanford



Collaborators

Stanford

Ken Goodson

Stanford

Eric Pop

Stanford

Simon Wong

Stanford

Mehdi Asheghi

Collaborators

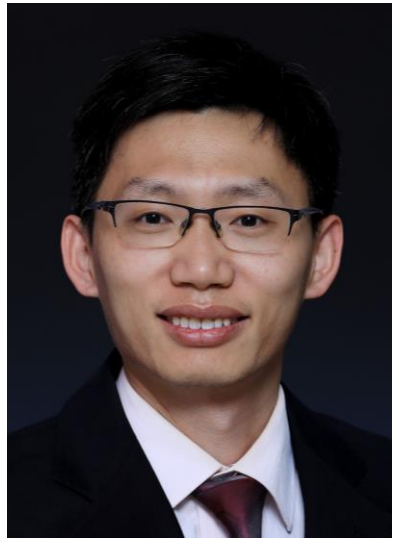
UC San Diego

Gert Cauwenberghs

清華大學 Tsinghua University

Huaqiang Wu

清華大學 Tsinghua University



Bin Gao

Stanford

Priyanka Raina

Collaborators

Stanford

Subhasish Mitra

Massachusetts Institute of Technology

Max Shulaker

NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE

Mohamed S. Aly

Stanford | SystemX Alliance

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Photo by Kasuma from Pexels