逻辑光刻工艺中的变量和不变量
（The Variables and Invariants in the Evolution of Logic Optical Lithography Process）

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内容提要（Outline）

- 简介 （Introduction）
- 光刻采用的主要技术一览 （Major Photolithographic Technologies at a Glance）
- 光刻工艺主要的新技术在不同逻辑技术节点上的引入和应用 （The Introduction and Application of Major New Technologies by Logic Technology Nodes）
- 评价光刻工艺的主要参数在不同逻辑技术节点上的引入和应用 （The Introduction and Application of Major Process Parameters by Logic Technology Nodes）
- 主要逻辑工艺技术节点的图像对比度和掩模版误差因子大小 （Image Contrast and Mask Error Factor for Major Logic Technology Nodes）
  - 栅极层工艺在主要逻辑技术节点的能量宽裕度 （Gate Layer Exposure Latitude from Major Logic Technology Nodes）
  - 栅极层工艺在主要逻辑技术节点的掩模版误差因子 （Gate Layer Mask Error Factor from Major Logic Technology Nodes）
  - 金属 1 层工艺在主要逻辑技术节点的能量宽裕度 （Metal 1 Layer Exposure Latitude from Major Logic Technology Nodes）
  - 金属 1 层工艺在主要逻辑技术节点的掩模版误差因子 （Metal 1 Layer Mask Error Factor from Major Logic Technology Nodes）
- 对比度的定义及其跟曝光能量宽裕度的关系 （Definition of Contrast and Its Relation with Exposure Latitude）
  - 黑白图像的对比度 （Contrast for B/W Patterns）
  - 彩色图像的对比度 （Contrast in Color Pictures）
- 主要逻辑工艺技术节点对栅极层线宽均匀性要求 （CDU Requirement for the Gate Layer at Major Logic Technology Nodes）
  - 对掩模版线宽均匀性的要求（CDU requirement for photomasks）
- 结论 Summary

简介（Introduction）

- 从0.25 微米到 7 nm技术节点，关键线宽从250 nm缩小到约20 nm，**约12.5倍**。但是成像所用的波长却从248 nm缩小到约134.7 nm（水浸没式193 nm光刻），不到50%。

  From 0.25 μm to 7 nm, the feature size has been shrinking by **12.5 times**. However, the imaging wavelength has only been shrunk from 248 nm to 134 nm (193 nm water immersion), less than a factor of 2.

- 为了实现这样具有挑战性的任务，光刻工艺先后发明了大量新技术和新方法，并得到了有效的使用。因此，光刻的做法也持续发生着很大的变化。

  In order to accomplish this, many new technologies and methods have been invented and put to effective use. Therefore, the methodology of photolithography is constantly changing significantly.

- 不过，光刻工艺中也有不变量，我们来一起看一下是哪些。

  But there are invariants, we will discuss them today.

光刻采用的主要技术一览 （Major Photolithographic Technologies at a Glance）

曝光设备 Exposure Tools

成像/照明 Imaging/Illumination

- 离轴照明Off-axis illumination
- 高数值孔径，水浸没Higher NA projection optics, water immersion
- 连续可调照明角度Continuous varying illumination angle
- 机载像差测量干涉仪 On-board interferometer for better lens aberration control
- 偏振照明 Polarization imaging
- 像素化照明 Pixelated illumination (Flexray)
- 照明激光带宽控制 Illumination laser bandwidth control

套刻/对准/对焦 Overlay/Alignment/Focus

- 离轴硅片对准 Off-axis wafer alignment/more complex lens
- 基于衍射的对准，套刻，和对焦 Diffraction based alignment, overlay, focus
- 更加准确的调平：气压阻滞测量，紫外照明调平 More accurate leveling: AGILE, UV leveling illumination
- 格点测绘 Gridmapping for better overlay

产能/使用/精度 Productivity/Utilization/Precision

- 暗场掩模版/掩模版受热套刻补偿 Smaller feature/Less transparent mask/Reticle heating correction
- 双工件台/更精密对准对时间的需求 Twin stage/Requirement for more time for sampling process induced overlay
- 串列工件台，产能提升 Tandem stage for throughput improvement
- 负显影/明场掩模版/镜头热效应补偿 NTD/Bright field mask/Lens heating correction
- 硅片范围线宽分布测量和调整， 更好的均匀性 Wafer level linewidth mapping and tuning for better CDU

光刻胶/抗反射层 Photoresist/Anti-Reflection Coatings

- 化学放大型光刻胶 Chemically amplified photoresist
- 低去保护活化能光刻胶 Low activation energy deprotection resist
- 抗反射层 Anti-reflection coating
- 双层抗反射层 Tri-layer imaging stack
- 精确地测量光酸扩散长度及其缩小路线图 Accurate measurement of photoacid diffusion length and its shrink roadmap
- 负显影 Negative toned developing

光掩模版 Photomask

- 邻近效应/雾化补偿 Proximity correction/fogging correction
- 亚分辨辅助图形 Sub-resolution assist features, serifs
- 相移掩模版 Phase shifting mask
- 薄二元掩模版 OMOG mask
- 更加薄的铬层，更好的图形保真度 Thinner chrome for better fidelity
- 掩模版工艺补偿 Mask process correction (MPC)
- 图形库伦效应补偿 Pattern Coulomb effect correction

工艺/涂胶-显影/刻蚀 Process/Track/Etch

- 显影/冲洗技术的发展 Evolution of developing/rinse methods
- 图形缩小的方法 Pattern trim/shrink methods
- 曝光后烘焙调节，光学邻近效应匹配 Post-exposure bake tuning for OPE matching
- 刻蚀线宽均匀性控制 Etch CDU control methods
- 多重图形技术 Multiple patterning methods

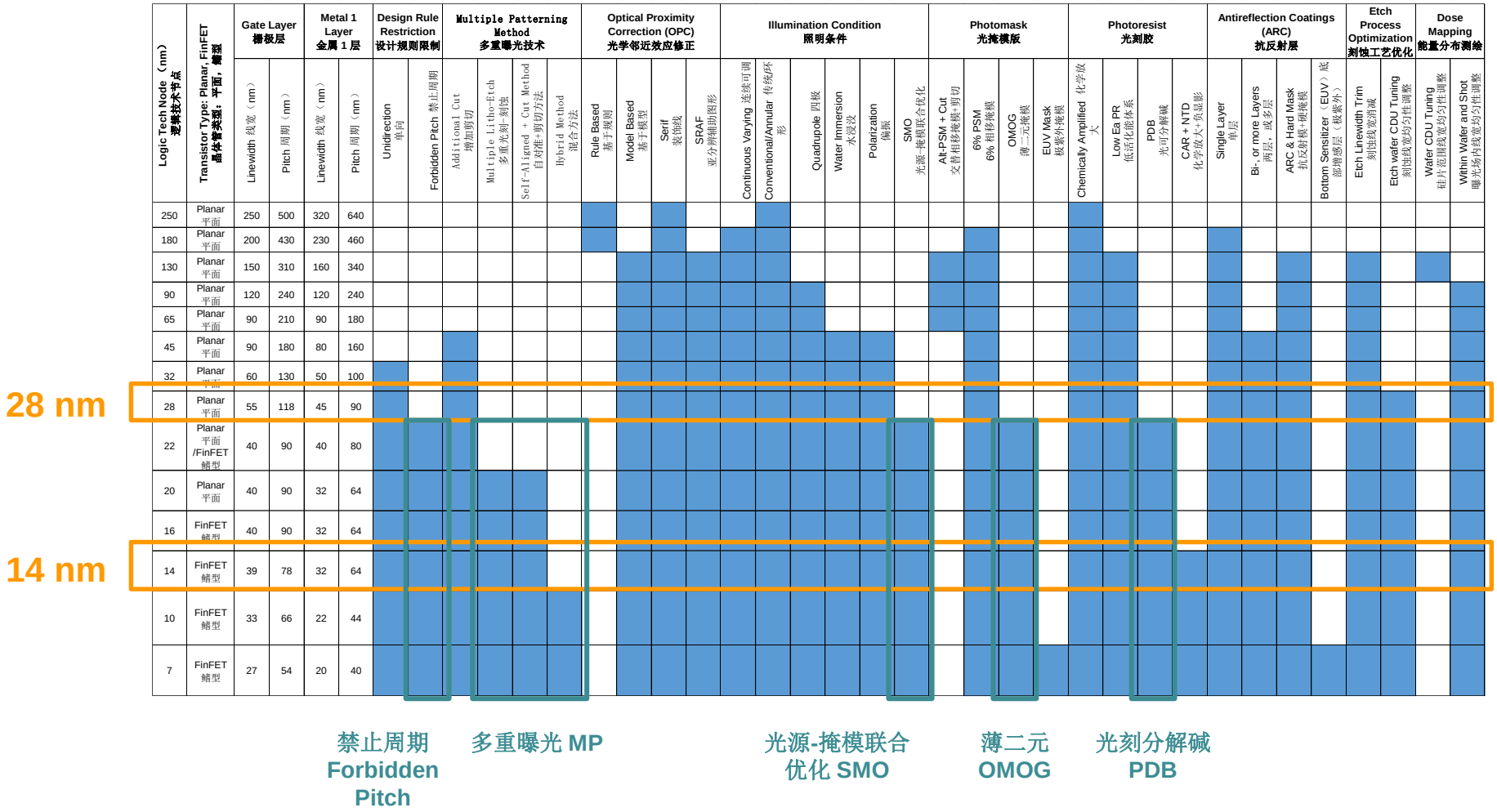
成像仿真，光学邻近效应修正 Image Simulation, Optical Proximity Correction (OPC)

- 霍普金斯理论体系下的光学邻近效应修正 Optical proximity correction (OPC) with Hopkins formulation (TCC)
- 光刻胶工艺仿真/整合参量模型 Photoresist process modeling (Developing, PEB)/Lumped parameter model (LPM)
- 带有矢量的传输交叉系数算法 Vector TCC algorithm
- 刻蚀偏置/负载效应仿真 Etch bias/loading effect modeling
- 掩模版三维散射仿真 Mask 3D scattering modeling
- 光刻胶三维形貌仿真 Resist 3D modeling
- 负显影工艺仿真 Negative tone developing (NTD) modeling
- 光源-掩模联合优化，更好地支持设计规则 Source-mask co-optimization (SMO) for better design rule support
- 极紫外掩模阴影效应/三维散射仿真 EUV mask shadowing effect/3D scattering modeling

设计规则 Design Rules

- 限制性设计规则/单向设计/禁止周期 Restricted design rules/uni-directional design/forbidden pitches
- 规范化的设计 Regularized design
- 可制造性设计 Design for manufacturing (DFM)
- 设计工艺协同优化 Design-technology co-optimization (DTCO)

光刻工艺主要的新技术在不同逻辑技术节点上的引入和应用
（The Introduction and Application of Major New Technologies by Logic Technology Nodes）



Logic Tech Node（nm） 逻辑技术节点	Transistor Type: Planar, FinFET 晶体管类型：平面，鳍型	Gate Layer 栅极层		Metal 1 Layer 金属 1 层		Design Rule Restriction 设计规则限制		Multiple Patterning Method 多重曝光技术				Optical Proximity Correction (OPC) 光学邻近效应修正				Illumination Condition 照明条件					Photomask 光掩模版				Photoresist 光刻胶				Antireflection Coatings (ARC) 抗反射层				Etch Process Optimization 刻蚀工艺优化		Dose Mapping 能量分布测绘	
		Linewidth 线宽（nm）	Pitch 周期（nm）	Linewidth 线宽（nm）	Pitch 周期（nm）	Unidirection 单向	Forbidden Pitch 禁止周期	Additional Cut 增加剪切	Multiple Litho-Etch 多重光刻-刻蚀	Self-Aligned + Cut Method 自对准+剪切方法	Hybrid Method 混合方法	Rule Based 基于规则	Model Based 基于模型	Serif 装饰线	SRAF 亚分辨辅助图形	Continuous Varying 连续可调	Conventional/Annular 传统/环形	Quadrupole 四极	Water Immersion 水浸没	Polarization 偏振	SMO 光源-掩模联合优化	Alt-PSM + Cut 交替相移掩模+剪切	6% PSM 6% 相移掩模	OMOG 薄二元掩模	EUV Mask 极紫外掩模	Chemically Amplified 化学放大	Low Ea PR 低活化能体系	PDB 光可分解碱	CAR + NTD 化学放大+负显影	Single Layer 单层	Bi-, or more Layers 两层，或多层	ARC & Hard Mask 抗反射膜+硬掩模	Bottom Sensitizer（EUV）底部增感层（极紫外）	Etch Linewidth Trim 刻蚀线宽消减	Etch wafer CDU Tuning 刻蚀线宽均匀性调整	Wafer CDU Tuning 硅片范围线宽均匀性调整	Within Wafer and Shot 曝光场内线宽均匀性调整
250	Planar 平面	250	500	320	640							■		■			■								■										
180	Planar 平面	200	430	230	460							■		■		■	■					■			■				■						
130	Planar 平面	150	310	160	340								■	■	■	■	■					■	■			■	■			■		■		■	
90	Planar 平面	120	240	120	240								■	■	■	■	■	■				■	■			■	■			■		■			■
65	Planar 平面	90	210	90	180								■	■	■	■	■					■	■			■	■			■		■			■
45	Planar 平面	90	180	80	160			■					■	■	■	■	■	■	■	■			■			■	■			■	■	■			■
32	Planar 平面	60	130	50	100	■		■					■	■	■	■	■	■	■	■			■			■	■			■	■	■			■
28	Planar 平面	55	118	45	90	■		■					■	■	■	■	■	■	■	■			■			■	■			■	■	■	■		■
22	Planar 平面 /FinFET 鳍型	40	90	40	80	■	■	■					■	■	■	■	■	■	■	■	■		■	■		■	■	■		■	■	■	■		■
20	Planar 平面	40	90	32	64	■	■	■	■	■			■	■	■	■	■	■	■	■	■		■	■		■	■	■		■	■	■	■		■
16	FinFET 鳍型	40	90	32	64	■	■	■	■	■			■	■	■	■	■	■	■	■	■		■	■		■	■	■		■	■	■	■		■
14	FinFET 鳍型	39	78	32	64	■	■	■	■	■			■	■	■	■	■	■	■	■	■		■	■		■	■	■	■	■	■	■	■		■
10	FinFET 鳍型	33	66	22	44	■	■	■	■	■	■		■	■	■	■	■	■	■	■	■		■	■		■	■	■	■	■	■	■	■		■
7	FinFET 鳍型	27	54	20	40	■	■	■	■	■	■		■	■	■	■	■	■	■	■	■		■	■		■	■	■	■	■	■	■	■		■

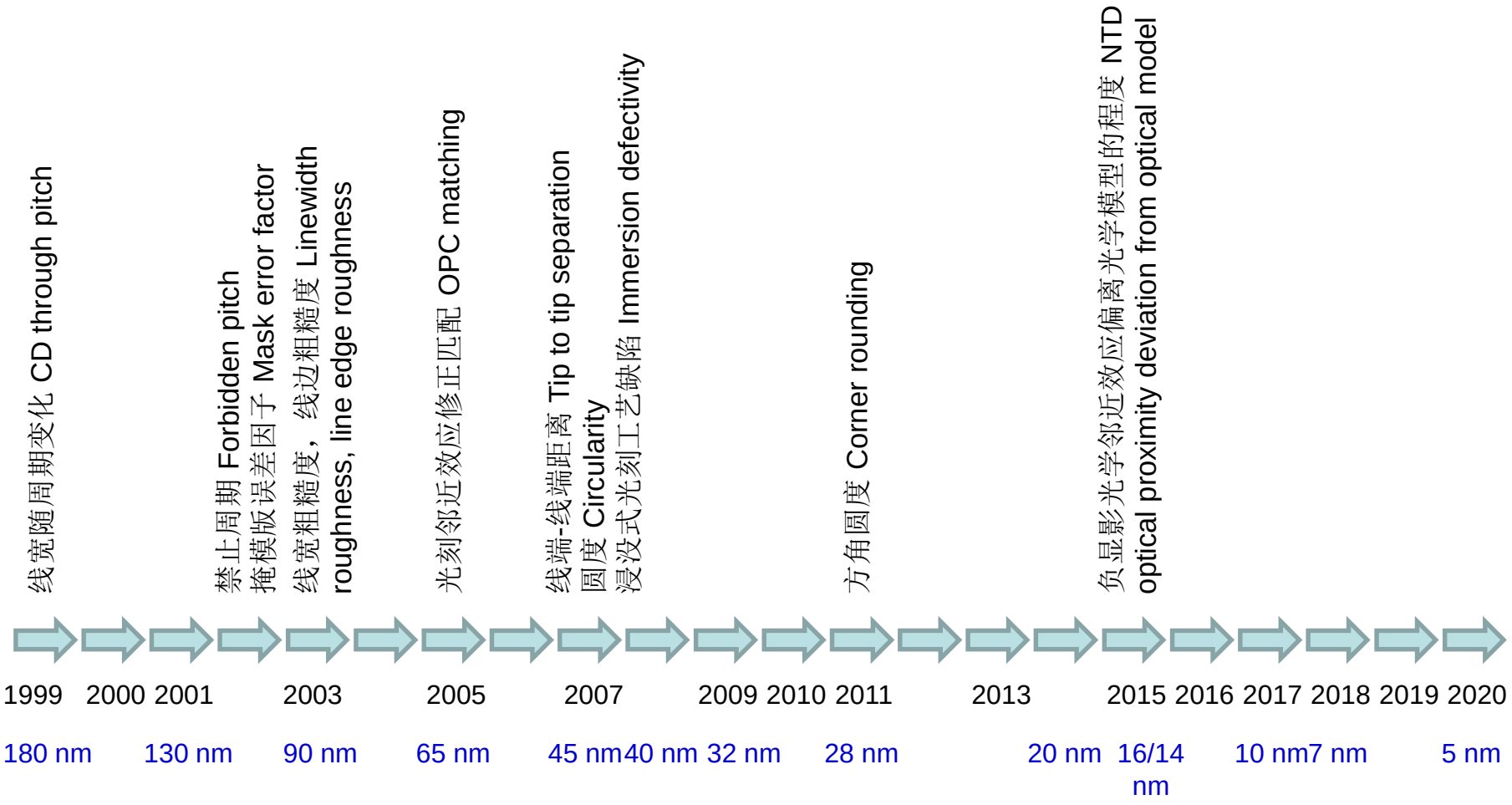
传统参数 Traditional Parameters

- 曝光能量宽裕度/焦深 Exposure Latitude/Depth of focus
- 光刻胶抗刻蚀能力/厚度/厚度均匀性 Photoresist etch resistance/thickness/thickness uniformity
- 光刻胶断面形貌 Photoresist cross sectional profile
- 芯片范围/硅片范围线宽均匀性 Across chip/across wafer linewidth variation
- 图形方角变圆程度 Pattern corner rounding

增加参数 Added Parameters

- 线宽随周期变化 CD through pitch (~1999, 180 nm 技术节点 technology node)
- 禁止周期 Forbidden pitch (2002, 110 nm 技术节点 technology node)
- 掩模版误差因子 Mask error factor (2002, 110 nm 技术节点 technology node)
- 线宽粗糙度，线边粗糙度 Linewidth roughness, line edge roughness (~2003, 90 nm 技术节点 technology node)
- 光刻邻近效应修正匹配 OPC matching (~2005, 65 nm 技术节点 technology node)
- 线端-线端距离 Tip to tip separation (2007, 45 nm 技术节点 technology node)
- 圆度 Circularity (~2007, 45 nm 技术节点 technology node)
- 浸没式光刻工艺缺陷 Immersion defectivity (2007, 45 nm 技术节点 technology node)
- 方角圆度 Corner rounding (2011，28 nm 技术节点 technology node)
- 负显影光学邻近效应偏离光学模型的程度 NTD optical proximity deviation from optical model (2015, 14 nm 技术节点 technology node)

评价光刻工艺的主要参数在不同逻辑技术节点上的引入和应用
The Introduction and Application of Major Process Parameters by Logic Technology Nodes）



主要逻辑工艺技术节点的图像对比度和掩模版误差因子大小
（Image Contrast and Mask Error Factor for Major Logic Technology Nodes）

Logic Tech Node（nm） 逻辑技术节点	Transistor Type: Planar, FinFET 晶体管类型：平面，鳍型	Gate Layer 栅极层									Metal 1 Layer 金属 1 层									
		Mask: Binary/6% PSM/OMOG 掩模版：二元/6% 相移/薄二元	Photoresist Thickness（nm） 光刻胶厚度（nm）	Linewidth 线宽（nm）	Pitch 周期（nm）	Wavelength（nm）/Polarization 波长（nm）/偏振	Photoacid Diffusion Length（nm） 光酸扩散长度（nm）	Illumination Condition 照明条件	Exposure Latitude (EL) 曝光能量宽裕度	Mask Error Factor (MEF) 掩模版误差因子	Trench/Line 沟槽/线条	Mask: Binary/6% PSM/OMOG 掩模版：二元/6% 相移/薄二元	Photoresist Thickness（nm） 光刻胶厚度（nm）	Linewidth 线宽（nm）	Pitch 周期（nm）	Wavelength（nm）/Polarization 波长（nm）/偏振	Photoacid Diffusion Length（nm） 光酸扩散长度（nm）	Illumination Condition 照明条件	Exposure Latitude (EL) 曝光能量宽裕度	Mask Error Factor (MEF) 掩模版误差因子
250	Planar 平面	Binary 二元	700	250	500	248	70	0.55NA/Conventional 传统	19.3	1.47	Line 线条	Binary 二元	1000	320	640	248	70	0.55NA/Conventional 传统	29.3	1.03
180	Planar 平面	6% PSM 6% 相移	500	180	430	248	60	0.65NA/Annular 环形	17.7	1.39	Line 线条	6% PSM 6% 相移	600	230	460	248	70	0.60NA/Annular 环形	18.1	1.85
130	Planar 平面	6% PSM 6% 相移	400	150	310	248	30	0.70NA/Annular 环形	18.9	1.66	Trench （Copper）沟槽 （铜线引入）	6% PSM 6% 相移	400	160	340	248	30	0.70NA/Annular 环形	19.8	1.69
90	Planar 平面	6% PSM 6% 相移	300	120	240	193	25	0.70NA/Annular 环形	19.7	1.56	Trench 沟槽	6% PSM 6% 相移	300	120	240	193	30	0.70NA/Annular 环形	16.9	2
65	Planar 平面	6% PSM 6% 相移	220	90	210	193	20	0.85NA/Annular 环形	18.6	1.51	Trench 沟槽	6% PSM 6% 相移	200	90	180	193	20	0.75NA/Annular 环形	13.4	2.85
45	Planar 平面	6% PSM 6% 相移	200	90	180	193 immersion /XY pol 浸没/XY偏振	15	1.1NA/Annular 环形	22.5	1.51	Trench 沟槽	6% PSM 6% 相移	180	80	160	193 immersion /XY pol 浸没/XY偏振	15	1.1NA/Annular 环形	14.9	2.63
32	Planar 平面	6% PSM 6% 相移	110	60	130	193 immersion /XY pol 浸没/XY偏振	15	1.25NA/Weak DP 弱二极	18.95	1.47	Trench 沟槽	6% PSM 6% 相移	110	50	100	193 immersion /XY pol 浸没/XY偏振	15	1.25NA/CQ 交叉四极	11.9	3.5
28	Planar 平面	6% PSM 6% 相移	110	55	118	193 immersion /XY pol 浸没/XY偏振	10	1.35NA/Weak DP 弱二极	21.5	1.4	Trench 沟槽	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	10	1.35NA/CQ 交叉四极	12.6	3.2
22	Planar 平面 /FinFET 鳍型	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	22.6	1.45	Trench 沟槽	OMOG 薄二元	70	40	80	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	8.9 (with PDB含PDB：12.7)	3.5
20	Planar 平面	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	22.6	1.45	Trench 沟槽	6% PSM 6% 相移	90	32	64（LE2，SE Pitch=90）二重光刻刻蚀，单次光刻周期=90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	12.6 (Pitch周期=90)	3.2 (Pitch周期=90)
16	FinFET 鳍型	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	22.6	1.45	Trench 沟槽	6% PSM 6% 相移	90	32	64（LE2，SE Pitch=90）二重光刻刻蚀，单次光刻周期=90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	12.6 (Pitch周期=90)	3.2 (Pitch周期=90)
14	FinFET 鳍型	OMOG 薄二元	70	39	78/84	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Strong DP/SMO 强二极/光源-掩模联合优化	13.7/23.1	2.8/1.47	Line-NTD 线条-负显影	6% PSM 6% 相移	70	32	64（LE2，SE Pitch=90）二重光刻刻蚀，单次光刻周期=90	193 immersion /XY pol 浸没/XY偏振	10	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	9.63 (with PDB含PDB：13.98) （Pitch周期=90）	3.58 (Pitch周期=90)
10	FinFET 鳍型	6% PSM6% 相移	70	33	66 （SADP+Cut+LE） 自对准双重+剪切+单次	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	16.2/24.3 (Pitch周期=90/132）	3.1/1.1 (Pitch周期=90/132）	Line-NTD 线条-负显影	6% PSM 6% 相移	70	22	44（LESLE+Cut） 自对准辅助二重光刻刻蚀	193 immersion /XY pol 浸没/XY偏振	7	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	12.55 (Pitch周期=88)	3.35 (Pitch周期=88)
7	FinFET 鳍型	6% PSM 6% 相移	70	27	54 (SADP+Cut+LE) 自对准双重+剪切+单次	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	19.9/25.4 (Pitch周期=90/108）	2.3/1.22 (Pitch周期=90/108）	Trench 沟槽	OMOG 薄二元	70	20	40（LE2,SE Pitch=80）二重光刻刻蚀，单次光刻周期=80	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	8.9 (with PDB含PDB：12.7) (Pitch周期=80)	3.5 (Pitch周期=80)

主要逻辑工艺技术节点的图像对比度和掩模版误差因子大小
（Image Contrast and Mask Error Factor for Major Logic Technology Nodes）

传统/环形 Conventional /Annular

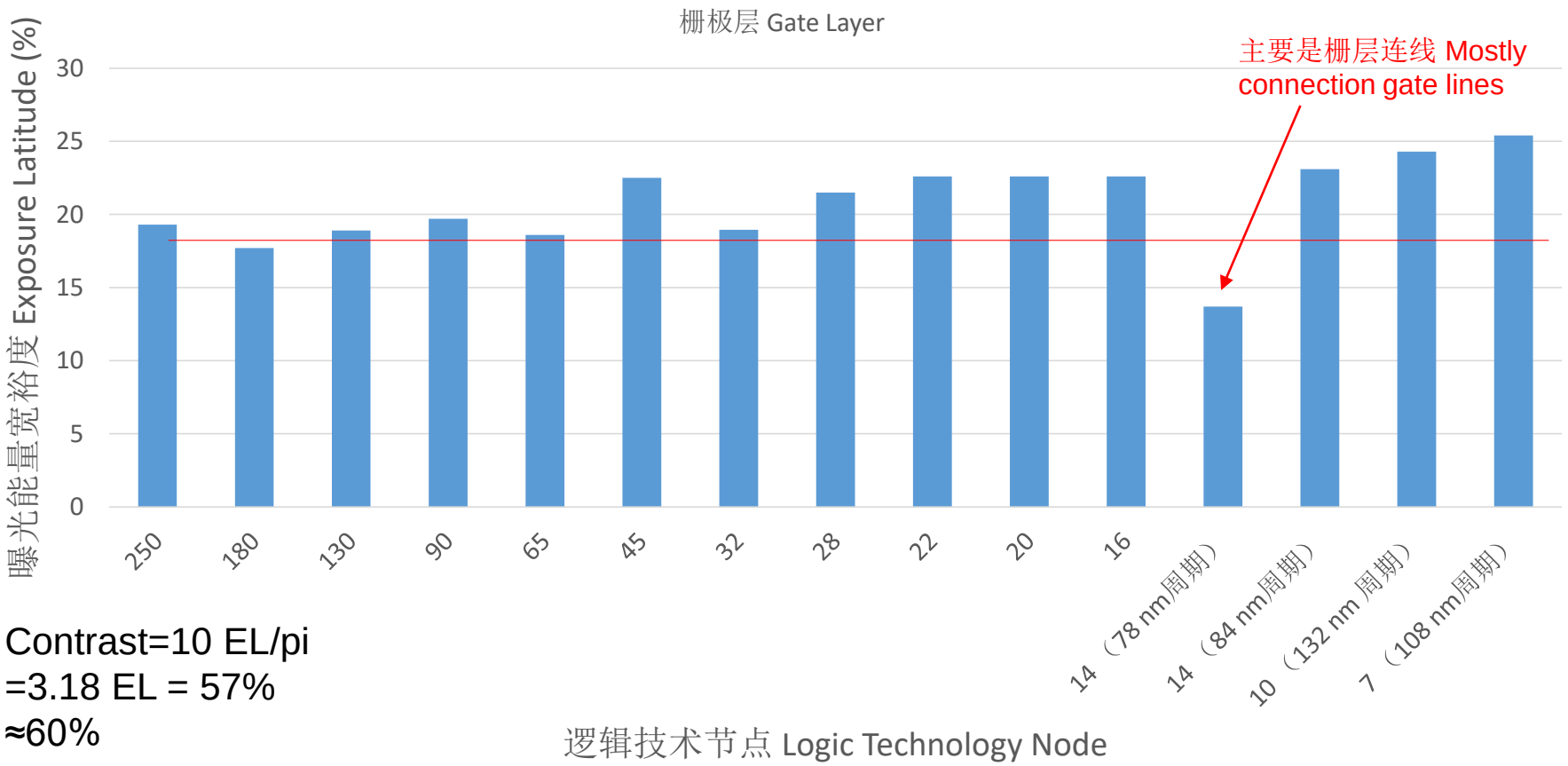
四极/二极 Quadrupole /Dipole

像素化Pixelated （SMO）

Logic Tech Node（nm）逻辑技术节点	Transistor Type: Planar, FinFET 晶体管类型：平面，鳍型	Gate Layer 栅极层									Metal 1 Layer 金属 1 层									
		Mask：Binary/6% PSM/OMOG 掩模版：二元/6% 相移/薄二元	Photoresist Thickness（nm）光刻胶厚度（nm）	Linewidth 线宽（nm）	Pitch 周期（nm）	Wavelength（nm）/Polarization 波长（nm）/偏振	Photoacid Diffusion Length（nm）光酸扩散长度（nm）	Illumination Condition 照明条件	Exposure Latitude (EL) 曝光能量宽裕度	Mask Error Factor (MEF) 掩模版误差因子	Trench/Line 沟槽/线条	Mask：Binary/6% PSM/OMOG 掩模版：二元/6% 相移/薄二元	Photoresist Thickness（nm）光刻胶厚度（nm）	Linewidth 线宽（nm）	Pitch 周期（nm）	Wavelength（nm）/Polarization 波长（nm）/偏振	Photoacid Diffusion Length（nm）光酸扩散长度（nm）	Illumination Condition 照明条件	Exposure Latitude (EL) 曝光能量宽裕度	Mask Error Factor (MEF) 掩模版误差因子
250	Planar 平面	Binary 二元	700	250	500	248	70	0.55NA/Conventional 传统	19.3	1.47	Line 线条	Binary 二元	1000	320	640	248	70	0.55NA/Conventional 传统	29.3	1.03
180	Planar 平面	6% PSM 6% 相移	500	180	430	248	60	0.65NA/Annular 环形	17.7	1.39	Line 线条	6% PSM 6% 相移	600	230	460	248	70	0.60NA/Annular 环形	18.1	1.85
130	Planar 平面	6% PSM 6% 相移	400	150	310	248	30	0.70NA/Annular 环形	18.9	1.66	Trench（Copper）沟槽（铜线引入）	6% PSM 6% 相移	400	160	340	248	30	0.70NA/Annular 环形	19.8	1.69
90	Planar 平面	6% PSM 6% 相移	300	120	240	193	25	0.70NA/Annular 环形	19.7	1.56	Trench 沟槽	6% PSM 6% 相移	300	120	240	193	30	0.70NA/Annular 环形	16.9	2
65	Planar 平面	6% PSM 6% 相移	220	90	210	193	20	0.85NA/Annular 环形	18.6	1.51	Trench 沟槽	6% PSM 6% 相移	200	90	180	193	20	0.75NA/Annular 环形	13.4	2.85
45	Planar 平面	6% PSM 6% 相移	200	90	180	193 immersion /XY pol 浸没/XY偏振	15	1.1NA/Annular 环形	22.5	1.51	Trench 沟槽	6% PSM 6% 相移	180	80	160	193 immersion /XY pol 浸没/XY偏振	15	1.1NA/Annular 环形	14.9	2.63
32	Planar 平面	6% PSM 6% 相移	110	60	130	193 immersion /XY pol 浸没/XY偏振	15	1.25NA/Weak DP 弱二极	18.95	1.47	Trench 沟槽	6% PSM 6% 相移	110	50	100	193 immersion /XY pol 浸没/XY偏振	15	1.25NA/CQ 交叉四极	11.9	3.5
28	Planar 平面	6% PSM 6% 相移	110	55	118	193 immersion /XY pol 浸没/XY偏振	10	1.35NA/Weak DP 弱二极	21.5	1.4	Trench 沟槽	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	10	1.35NA/CQ 交叉四极	12.6	3.2
22	Planar 平面 /FinFET 鳍型	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	22.6	1.45	Trench 沟槽	OMOG 薄二元	70	40	80	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	8.9 (with PDB含PDB：12.7)	3.5
20	Planar 平面	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	22.6	1.45	Trench 沟槽	6% PSM 6% 相移	90	32	64（LE2，SE Pitch=90）二重光刻刻蚀，单次光刻周期=90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	12.6 (Pitch周期=90)	3.2 (Pitch周期=90)
16	FinFET 鳍型	6% PSM 6% 相移	90	45	90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	22.6	1.45	Trench 沟槽	6% PSM 6% 相移	90	32	64（LE2，SE Pitch=90）二重光刻刻蚀，单次光刻周期=90	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	12.6 (Pitch周期=90)	3.2 (Pitch周期=90)
14	FinFET 鳍型	OMOG 薄二元	70	39	78/84	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Strong DP/SMO 强二极/光源-掩模联合优化	13.7/23.1	2.8/1.47	Line-NTD 线条-负显影	6% PSM 6% 相移	70	32	64（LE2，SE Pitch=90）二重光刻刻蚀，单次光刻周期=90	193 immersion /XY pol 浸没/XY偏振	10	1.35NA/CQ/SMO 交叉四极/光源-掩模联合优化	9.63 (with PDB含PDB：13.98)（Pitch周期=90）	3.58 (Pitch周期=90)
10	FinFET 鳍型	6% PSM6% 相移	70	33	66（SADP+Cut+LE）自对准双重+剪切+单次	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	16.2/24.3 (Pitch周期=90/132)	3.1/1.1 (Pitch周期=90/132)	Line-NTD 线条-负显影	6% PSM 6% 相移	70	22	44（LESLE+Cut）自对准辅助二重光刻刻蚀	193 immersion /XY pol 浸没/XY偏振	7	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	12.55 (Pitch周期=88)	3.35 (Pitch周期=88)
7	FinFET 鳍型	6% PSM 6% 相移	70	27	54 (SADP+Cut+LE) 自对准双重+剪切+单次	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	19.9/25.4 (Pitch周期=90/108)	2.3/1.22 (Pitch周期=90/108)	Trench 沟槽	OMOG 薄二元	70	20	40（LE2,SE Pitch=80）二重光刻刻蚀，单次光刻周期=80	193 immersion /XY pol 浸没/XY偏振	5	1.35NA/Weak DP/SMO 弱二极/光源-掩模联合优化	8.9 (with PDB含PDB：12.7) (Pitch周期=80)	3.5 (Pitch周期=80)

- 照明条件从传统/环形照明，逐渐发展为四极、二极、像素化（SMO）。 The exposure condition has been evolving from the conventional/annular gradually to quadrupoles, dipoles, and pixelated （SMO）

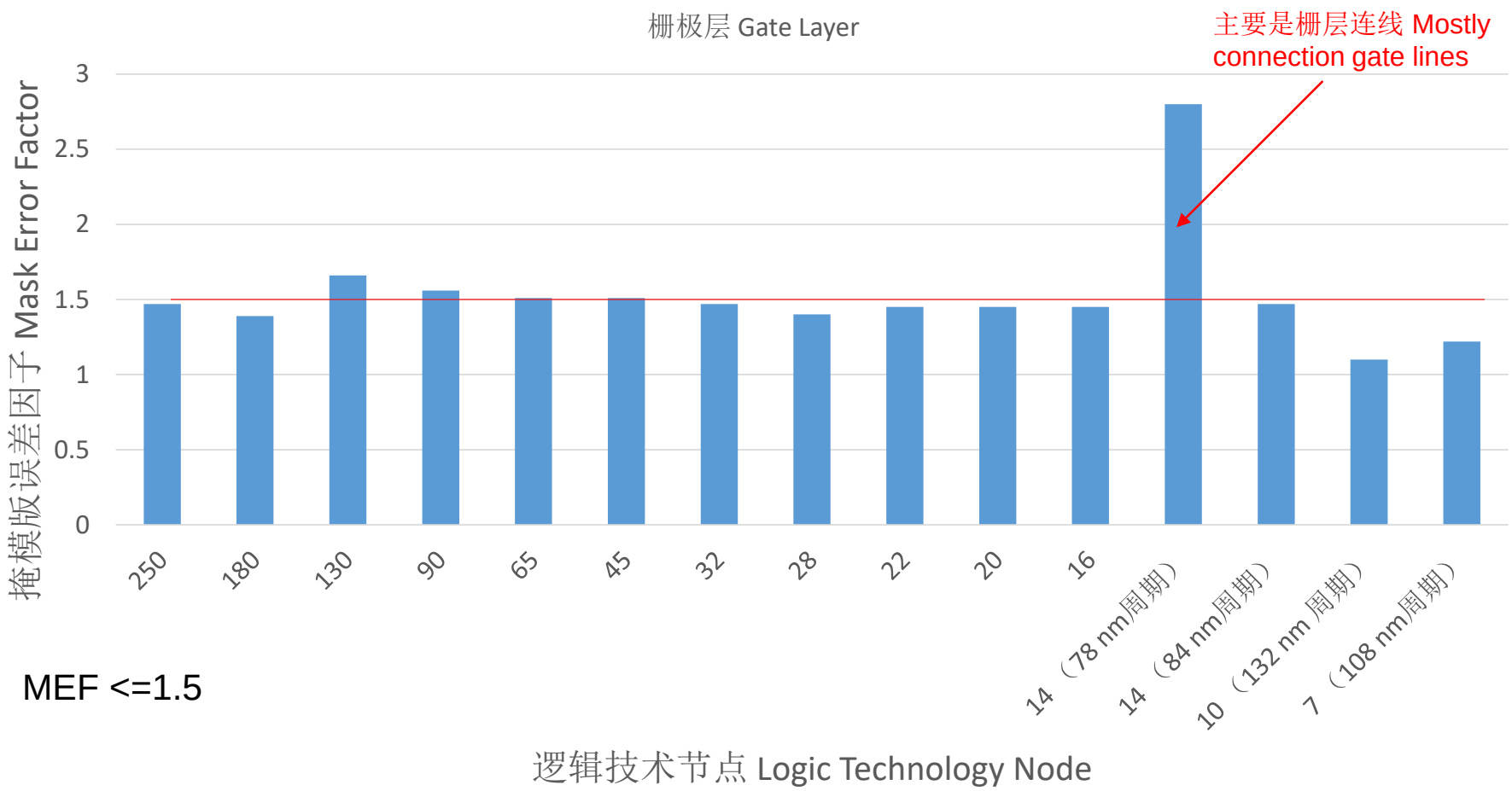
栅极层工艺在主要逻辑技术节点的能量宽裕度
（Gate Layer Exposure Latitude from Major Logic Technology Nodes）



Contrast=10 EL/pi
=3.18 EL = 57%
≈60%

- 绝大多数技术节点的栅极层曝光能量宽裕度在20% 或者更高。 The exposure latitudes for the Gate Layer at most technology nodes are at 20% or higher.

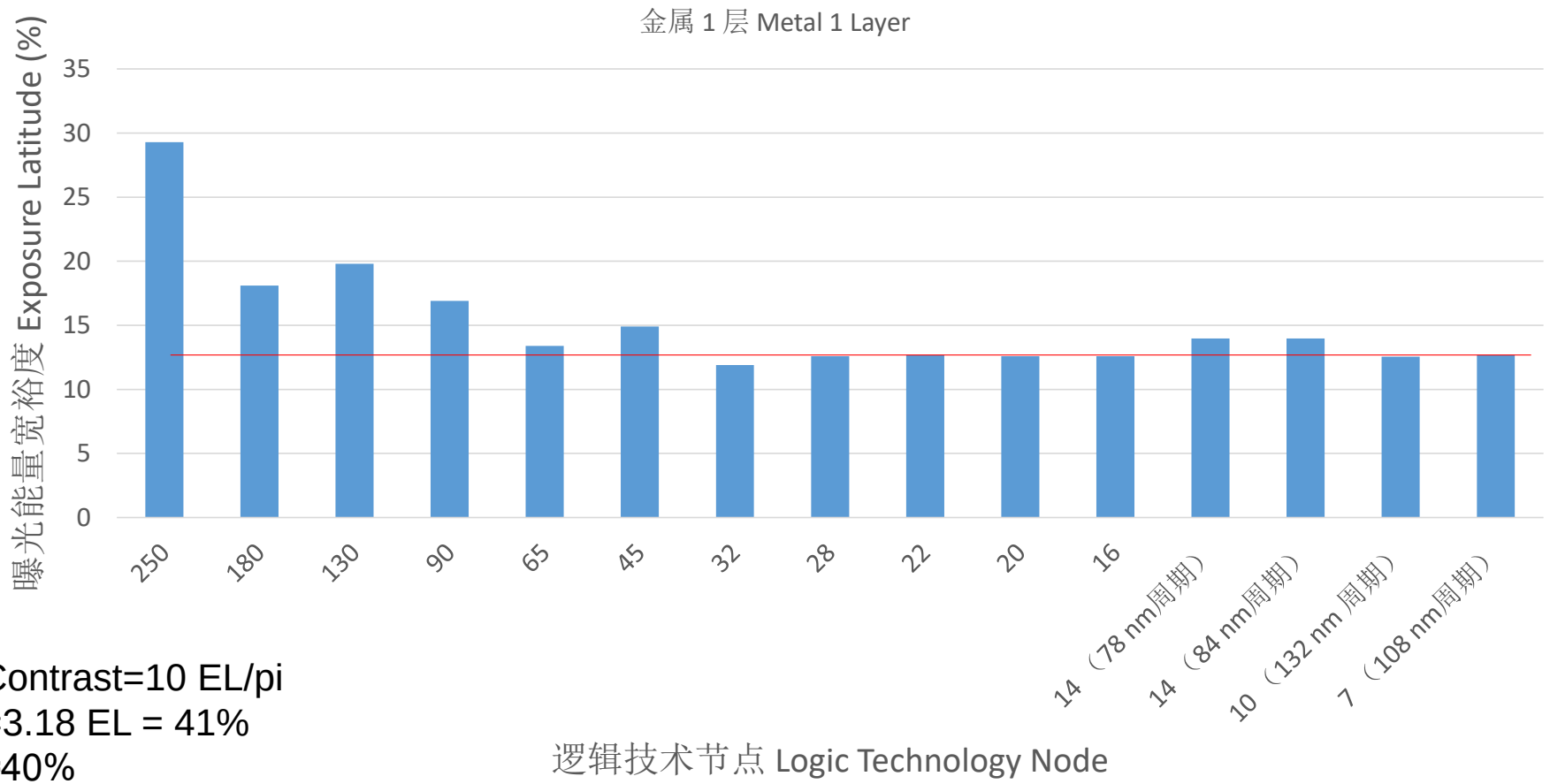
栅极层工艺在主要逻辑技术节点的掩模版误差因子
（Gate Layer Mask Error Factor from Major Logic Technology Nodes）



MEF <=1.5

- 绝大多数技术节点的栅极层掩模版误差因子在1.5以内。 The Mask Error Factor (MEF) for for the Gate Layer at most technology nodes are within 1.5.

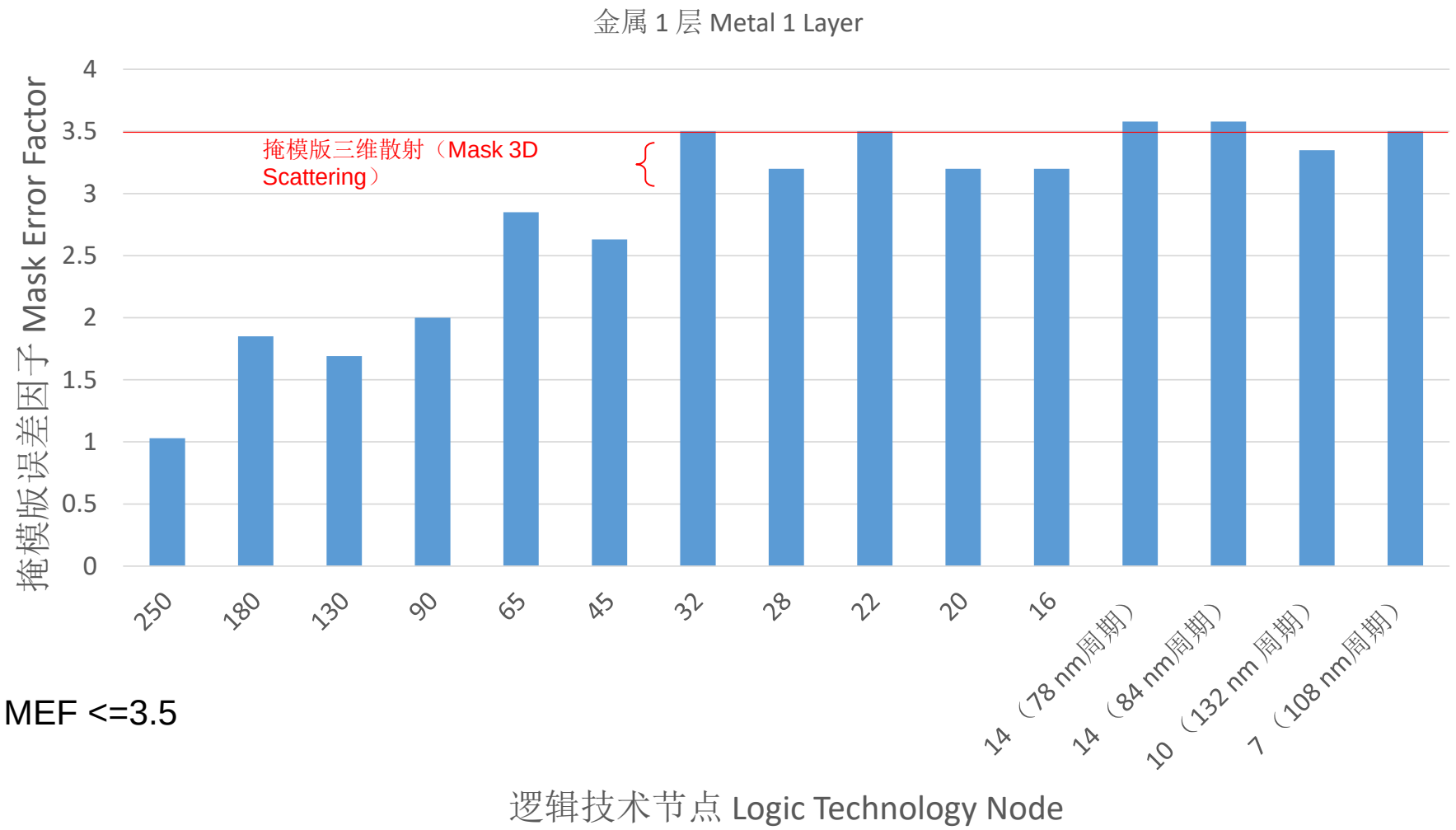
金属 1 层工艺在主要逻辑技术节点的能量宽裕度
（Metal 1 Layer Exposure Latitude from Major Logic Technology Nodes）



Contrast=10 EL/pi
=3.18 EL = 41%
≈40%

- 绝大多数技术节点的金属1层曝光能量宽裕度在13%或者更大。 The exposure latitudes for Metal 1 Layer at most technology nodes are at 13% or higher.

金属 1 层工艺在主要逻辑技术节点的掩模版误差因子
（Metal 1 Layer Mask Error Factor from Major Logic Technology Nodes）

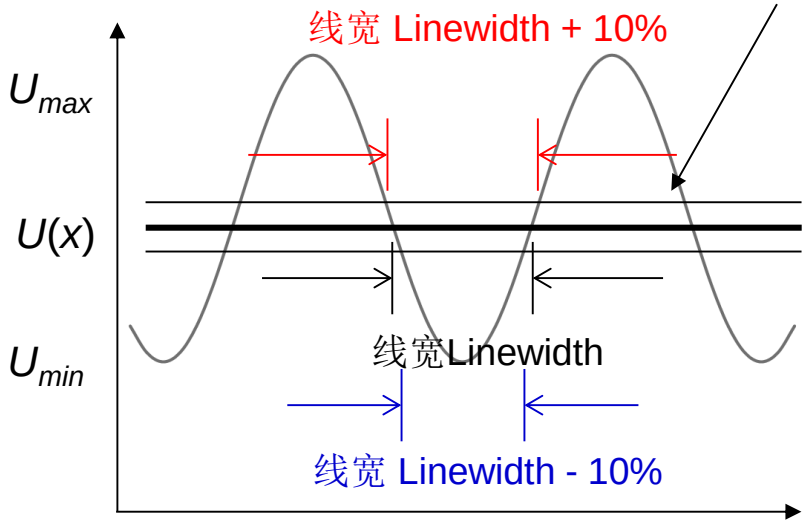


MEF <=3.5

- 绝大多数技术节点的金属 1 层掩模版误差因子在3.5以内。 The Mask Error Factor (MEF) for the Metal 1 Layer at most technology nodes are within 3.5.
- 掩模版三维散射导致误差因子上升约0.5到0.7之间。 The mask 3D scattering causes an extra 0.5 to 0.7 MEF increase.

对比度的定义及其跟曝光能量宽裕度的关系 （Definition of Contrast and Its Relation with Exposure Latitude）

空间像实际光强分布
Aerial image intensity



曝光能量宽裕度的定义：
Definition of Exposure Latitude（*EL*）：

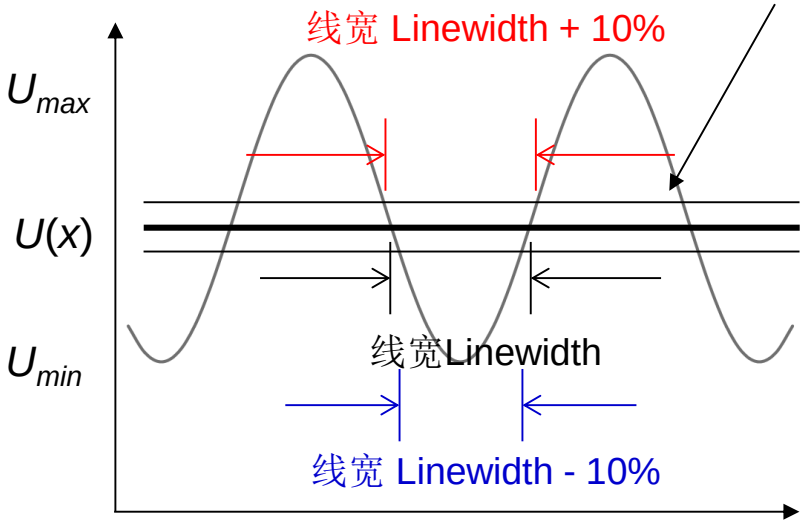
对于线宽等于+/-10%的情况下，曝光能量范围相对于曝光能量的比值
The ratio between exposure energy range （corresponding to the +/-10% linewidth）and the exposure energy

$$EL = \frac{\Delta E(corresponding\ to \pm 10\%\ linewidth)}{E}$$

$$U(x) = \frac{(U_{max}+U_{min})}{2} + \frac{(U_{max}-U_{min})}{2}\cos\left(\frac{2\pi x}{p}\right)$$

$$= U_0\left(1 + contrast\cos\left(\frac{2\pi x}{p}\right)\right)$$

空间像实际光强分布
Aerial image intensity



$$U(x) = \frac{(U_{max} + U_{min})}{2} + \frac{(U_{max} - U_{min})}{2}\cos\left(\frac{2\pi x}{p}\right)$$
$$= U_0\left(1 + contrast\ \cos\left(\frac{2\pi x}{p}\right)\right)$$

$$EL = \frac{\Delta E(correspond\ ing\ to \pm 10\%\ linewidth)}{E}$$
$$= \frac{1}{U_0}\left|\frac{dU(x)}{dx}\right|\Delta L = contrast\ \frac{2\pi}{p}\sin\left(\frac{2\pi L}{p}\right)\Delta L$$

当线宽*Linewidth*=周期*p*的一半（1/2）时，
U(*x*) =0，

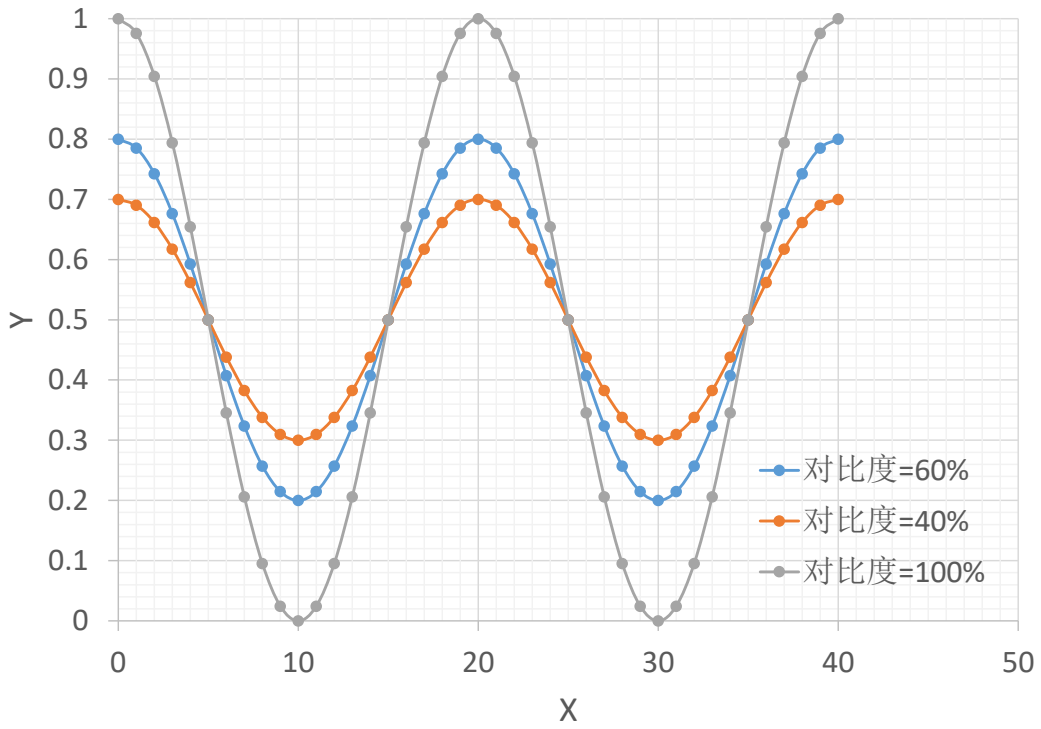
$$EL = 对比度（contrast）\frac{\Delta L}{L}\pi = \frac{\pi}{10}对比度（contrast），$$

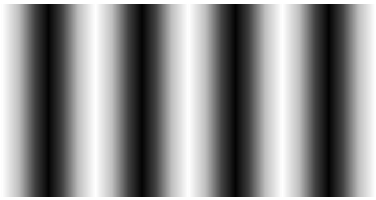
或

$$对比度（contrast）= \frac{L}{\Delta L}\frac{EL}{\pi} = \frac{10}{\pi}EL$$

L: *Linewidth*

黑白图像的对比度 （Contrast for B/W Patterns）



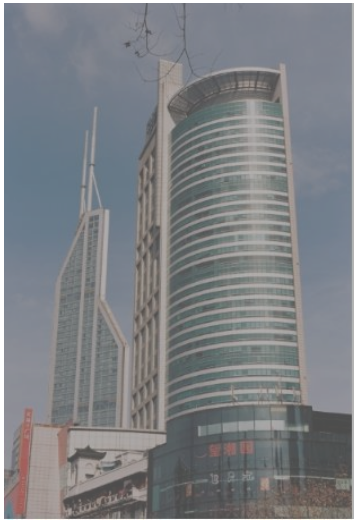
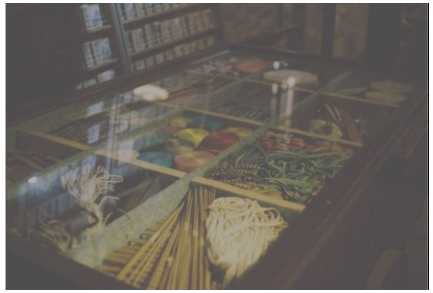
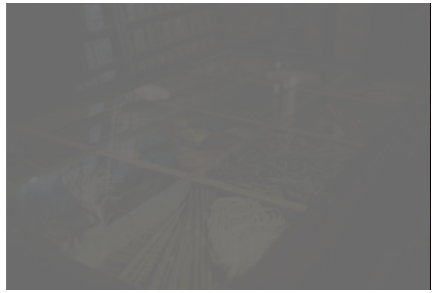


对比度
Contrast
=100%

对比度
Contrast
=60%

对比度
Contrast
=40%

彩色图像的对比度 （Contrast in Color Pictures）

	参考对比度（Reference contrast）=100%	栅极层的最低要求 （Min Contrast Required for Gate）: 60%	金属层的最低要求 （Min Contrast Required for Metal）: 40%	参考对比度（Reference contrast）=5%
明场（Bright Field） 海鸥DF-2ETM相机，凤凰18-28mm 镜头拍摄				
暗场（Dark Field） 华夏841相机40 mm镜头拍摄				

主要逻辑工艺技术节点对栅极层线宽均匀性要求
（CDU Requirement for the Gate Layer at Major Logic Technology Nodes）

生产年代 Year of Production	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
逻辑工艺技术节点 Logic Technology Node (nm)	**130**		**90**		**65**		**45**	**40**	**32**		**28**			**20**	**16/14**		**10**	**7**		**5**
逻辑半周期 Logic Half Pitch （ITRS2001)	150	130	107	90	80	70	65													
逻辑金属半周期 Logic Metal Half Pitch（ITRS2005）					90	78	68	59	52	45	40	36	32							
逻辑金属半周期 Logic Metal Half Pitch（ITRS2013）													40	32	32	28	25	23	20	18
逻辑代工半周期-金属1层 Foundry Half Pitch-Metal 1（nm）	170		120		90		80	60	50		45			32	32		22	20		16
逻辑代工半周期-栅极 Foundry Half Pitch-Gate（nm）	155		120		105		90	81	65		59			45	43.5		33	27		22
栅极物理线宽 Gate Physical CD (nm) ITRS 2001	65		45		32		25													
栅极物理线宽 Gate Physical CD (nm) ITRS 2005					32		25	23	20		16		13							
栅极物理线宽 Gate Physical CD (nm) ITRS 2013													20	18	17		14	13		11
线宽均匀性 CDU （3sigma,nm）ITRS 2001	5.3		3.7		2.6		2													
线宽均匀性 CDU （3sigma,nm）ITRS 2005					3.3		2.6	2.3	2.1		1.7		1.3							
线宽均匀性 CDU （3sigma,nm）ITRS 2013													2	1.8	1.7		1.4	1.3		1.1
线宽均匀性/栅极物理线宽 CDU/Gate Physical CD （%）	8.2%		8.2%		10.3%		10.4%	10.0%	10.5%		10.6%			10.0%	10.0%		10.0%	10.0%		10.0%
线宽均匀性/栅极半周期 CDU/Gate Half Pitch（%）	3.4%		3.1%		3.1%		2.9%	2.8%	3.2%		2.9%			4.0%	3.9%		4.2%	4.8%		5.0%

主要逻辑工艺技术节点对栅极层线宽均匀性要求
（CDU Requirement for the Gate Layer at Major Logic Technology Nodes）

生产年代 Year of Production	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
逻辑工艺技术节点 Logic Technology Node（nm）	**130**		**90**		**65**		**45**	**40**	**32**		**28**			**20**	**16/14**		**10**	**7**		**5**
逻辑半周期 Logic Half Pitch（ITRS2001）	150	130	107	90	80	70	65													
逻辑金属半周期 Logic Metal Half Pitch（ITRS2005）					90	78	68	59	52	45	40	36	32							
逻辑金属半周期 Logic Metal Half Pitch（ITRS2013）													40	32	32	28	25	23	20	18
逻辑代工半周期-金属1层 Foundry Half Pitch-Metal 1（nm）	170		120		90		80	60	50		45			32	32		22	20		16
逻辑代工半周期-栅极 Foundry Half Pitch-Gate（nm）	155		120		105		90	81	65		59			45	43.5		33	27		22
栅极物理线宽 Gate Physical CD（nm）ITRS 2001	65		45		32		25													
栅极物理线宽 Gate Physical CD（nm）ITRS 2005					32		25	23	20		16		13							
栅极物理线宽 Gate Physical CD（nm）ITRS 2013													20	18	17		14	13		11
线宽均匀性 CDU （3sigma,nm）ITRS 2001	5.3		3.7		2.6		2													
线宽均匀性 CDU （3sigma,nm）ITRS 2005					3.3		2.6	2.3	2.1		1.7		1.3							
线宽均匀性 CDU （3sigma,nm）ITRS 2013													2	1.8	1.7		1.4	1.3		1.1
线宽均匀性/栅极物理线宽 CDU/Gate Physical CD （%）	8.2%		8.2%		10.3%		10.4%	10.0%	10.5%		10.6%			10.0%	10.0%		10.0%	10.0%		10.0%
线宽均匀性/栅极半周期 CDU/Gate Half Pitch（%）	3.4%		3.1%		3.1%		2.9%	2.8%	3.2%		2.9%			4.0%	3.9%		4.2%	4.8%		5.0%

- 线宽均匀性控制要求相对于栅极的物理宽度的比例是几乎不变的，约+/-10%。The gate linewidth control tolerance relative to its physical linewidth is nearly constant, about +/-10%.

- 线宽均匀性控制要求相对于栅极层的半周期在*接近衍射极限时*从+/- 3%增加到+/- 4%，到了*双重曝光*后增加到+/-5%。 The gate linewidth control tolerance relative to gate half pitch increases as *the diffraction limit is approached* from +/- 3% to +/- 4%, and to +/-5% as *double patterning methods are used*.

主要逻辑工艺技术节点对栅极层线宽均匀性要求
（CDU Requirement for the Gate Layer at Major Logic Technology Nodes）

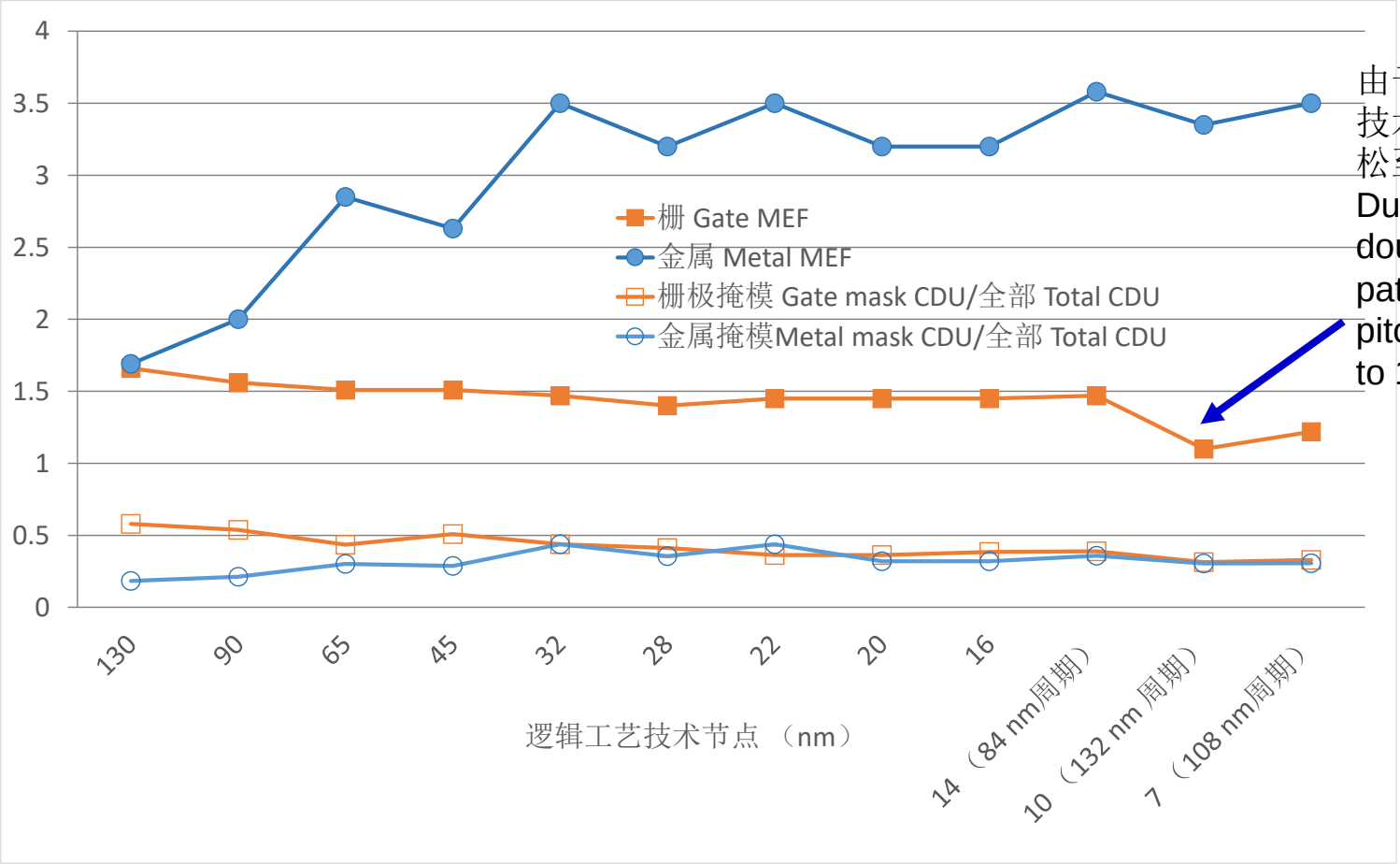
对掩模版线宽均匀性的要求（CDU requirement for photomasks）

生产年代 Year of Production	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
逻辑工艺技术节点 Logic Technology Node (nm)	130		90		65		45	40	32		28			20	16/14		10	7		5 非极紫外 (Non-EUV)
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2001 (Binary) (4X)	7.4		5.1		4.2		3.5													
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2005 (4X)					3.8		3.5	3	2.5		2		2							
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2013 (4X)													2	1.8	1.8		1.6	1.6		1.4
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2001 (Binary) (1X)	1.85		1.28		1.05		0.88													
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2005 (1X)					0.95		0.88	0.75	0.63		0.50		0.50							
掩模版线宽均匀性 CDU for Photomask Making (3sigma, nm) ITRS 2013 (1X)													0.50	0.45	0.45		0.40	0.40		0.35
线宽均匀性 CDU （3sigma,nm）ITRS 2001	5.3		3.7		2.6		2													
线宽均匀性 CDU （3sigma,nm）ITRS 2005					3.3		2.6	2.3	2.1		1.7		1.3							
线宽均匀性 CDU （3sigma,nm）ITRS 2013													2	1.8	1.7		1.4	1.3		1.1
掩模版线宽均匀性*MEF/全部线宽均匀性 Photomask Making CDU*MEF/Total CDU, ITRS 2001	0.52		0.52		0.61		0.66													
掩模版线宽均匀性*MEF/全部线宽均匀性 Photomask Making CDU*MEF/Total CDU, ITRS 2005					0.43		0.50	0.49	0.45		0.44		0.58							
掩模版线宽均匀性*MEF/全部线宽均匀性 Photomask Making CDU*MEF/Total CDU, ITRS 2013													0.38	0.38	0.40		0.43	0.46		0.48

- 掩模版的线宽均匀性参考ITRS的建议和实际电子束曝光机的能力 The mask making CDU references ITRS numbers and real world mask writer capabilities.

主要逻辑工艺技术节点对栅极层线宽均匀性要求
（CDU Requirement for the Gate Layer at Major Logic Technology Nodes）

对掩模版线宽均匀性的要求（CDU requirement for photomasks）



由于二重图形技术，周期放松至 132 nm
Due to double patterning，pitch relaxed to 132 nm

- 栅极层和金属层掩模版线宽均匀性预算（3倍标准偏差）所占全部线宽均匀性的40%-50%。The 3-sigma gate and metal layer mask CDU budget is about 40-50% of that of the total CDU.
- 金属层的掩模版误差因子在90 nm技术节点后开始显著增加。The MEF of the metal layer started to increase significantly at 90 nm technology node.

总结（Summary）

- 变量 Variables
  - 用来评价光刻工艺的参数 Parameters that are used for the photolithographic process evaluation
  - 被光刻工艺使用的各项技术 The technologies that are used by the photolithographic processes
  - 照明条件从传统/环形照明，逐渐发展为四极、二极、像素化（SMO） The exposure condition has been evolving from the conventional/annular gradually to quadrupoles, dipoles, and pixelated （SMO）
- 不变量/近似不变量 Invariants/Nearly Invariants：
  - 曝光能量宽裕度/对比度 Exposure Latitude/Imaging Contrast
  - 掩模版误差因子 Mask Error Factor （MEF）
  - 相对于栅极物理宽度的线宽均匀性控制要求 Percentage Linewidth Tolerance relative to Physical Gate Length
  - 相对于栅极层半周期的线宽均匀性控制要求 Percentage Linewidth Tolerance relative to Gate Layer Half Pitch
  - 掩模版线宽均匀性预算占整体线宽均匀性的比例：40%-50% The mask CDU budget is about 40-50% of that of the total CDU budget

Back up

2001 ITRS Roadmap

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM							
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
Contact in resist (nm)	165	140	130	110	100	90	80
Contact after etch (nm)	150	130	115	100	90	80	70
Overlay	46	40	35	32	28	25	23
CD control (3 sigma) (nm)	15.9	14.1	12.2	11.0	9.8	8.6	8.0
MPU							
MPU ½ Pitch (nm)	150	130	107	90	80	70	65
MPU gate in resist (nm)	90	70	65	53	45	40	35
MPU gate length after etch (nm)	65	53	45	37	32	28	25
Contact in resist (nm)	165	140	122	100	90	80	75
Contact after etch (nm)	150	130	107	90	80	70	65
Gate CD control (3 sigma) (nm)	5.3	4.3	3.7	3.0	2.6	2.4	2.0
ASIC/LP							
ASIC/LP ½ Pitch (nm)	150	130	107	90	80	70	65
ASIC/LP gate in resist (nm)	130	107	90	75	65	53	45
ASIC/LP gate length after etch (nm)	90	80	65	53	45	37	32
Contact in resist (nm)	165	140	122	100	90	80	75
Contact after etch (nm)	150	130	107	90	80	70	65
CD control (3 sigma) (nm)	7.3	6.5	5.3	4.3	3.7	3.0	2.6
Chip size (mm^2)							
DRAM, introduction	390	308	364	287	454	359	568
DRAM, production	127	100	118	93	147	116	183
MPU, high volume at introduction	280	280	280	280	280	280	280
MPU, high volume at production	140	140	140	140	140	140	140
MPU, high performance	310	310	310	310	310	310	310
ASIC	800	800	572	572	572	572	572
Minimum field area	800	800	572	572	572	572	572
Wafer size (diameter, mm)	300	300	300	300	300	300	300

White–Manufacturable Solutions Exist, and Are Being Optimized

Yellow--Manufacturable Solutions are Known

Red–Manufacturable Solutions are NOT Known

$$\frac{1}{U_0}\left|\frac{dU(x)}{dx}\right| = \frac{d\{\ln[U(x)]\}}{dx}$$

$$NILS = \frac{CD}{U(x)}\frac{dU(x)}{dx}$$

$$NILS = \pi\, contrast = EL\frac{CD}{dCD}$$

2005 ITRS Roadmap

Table 74 Various Techniques for Achieving Desired CD Control and Overlay with Optical Projection Lithography

MPU M1 contacted ½ pitch	*210 nm*	*160 nm*	*120 nm*	*90 nm*	*65 nm*	*45 nm*
k_1 Range [A]	*0.51–0.64*	*0.48–0.52*	*0.47–0.53*	*0.40–0.43*	*0.31–0.40*	*0.28–0.31*
Design rules	Minor restriction	Allow OPC and PSM, SRAF	Litho friendly design rules			
Restrictions (cumulative)	Minimum pitch, spacing and linewidth		Pitch and orientation	Contact locations, library cells checked for OPC compatibility and printability	Features on grid?, Restricted feature set?	
Masks (Optical proximity correction)	Rule-based OPC, MBOPC for gate, custom OPC for memory cells	Model-based OPC (MBOPC) on critical layers, SRAF on gate layer	Model-based OPC w /SRAF on critical layers, verification of entire corrected layout with simulation		Model-based OPC with vector simulation, SRAF, polarization corrections	Model-based OPC with vector simulation, SRAF, polarization corrections, variation of OPC intensity by location in circuit?, magnification increase?
(Gate and M1 layer mask type)		cPSM and EPSM		APSM, EPSM and hiT EPSM	APSM, hiT EPSM, dual dipole?	APSM, hiT EPSM, double exposure with 2× larger pitch
(Contacts/vias layers mask type)		EPSM		APSM, EPSM, HiT PSM		
Resist	Custom by layer type					
Thickness	<500 nm	<400 nm	<350 nm	<280 nm	<225 nm	<160 nm
Substrate	ARC	ARC, hard masks		ARC, hard masks, top coats		
Etch	Post development resist width reduction					
Tool		Selection based on aberrations, automated NA/sigma control		Aberration monitoring		
(Illumination)	Conventional, annular illumination	Off-axis illumination	Quadrupole	Custom illumination	Custom illumination, polarization optimization	Custom illumination, polarization optimization
(Dose control)		Cross wafer dose adjustments	Dose adjustment across the wafer and along scan			
(Process control (CD and overlay)	Offsets from previous lots	Automated process control with downloaded offsets			Automated process control with downloaded offsets, metrology integrated in lithography cell	

MBOPC—model based optical proximity correction cPSM—complementary PSM APSM—alternating PSM
EPSM—embedded PSM HiT—high transmission ARC—antireflection coating SRAF—sub-resolution assist features

Note for Table 74:
[A] Assumes that optical and immersion optical projection lithography is used.

Table 76a Lithography Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
DRAM and Flash									
DRAM ½ pitch (nm)	80	70	65	57	50	45	40	35	32
Flash ½ pitch (nm) (un-contacted poly)	76	64	57	51	45	40	36	32	28
Contact in resist (nm)	94	79	70	63	56	50	44	39	35
Contact after etch (nm)	85	72	64	57	51	45	40	36	32
Overlay [A] (3 sigma) (nm)	15	13	11	10	9	8	7.1	6.4	5.7
CD control (3 sigma) (nm) [B]	8.8	7.4	6.6	5.9	5.3	4.7	4.2	3.7	3.3
MPU									
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	90	78	68	59	52	45	40	36	32
MPU gate in resist (nm)	54	48	42	38	34	30	27	24	21
*MPU physical gate length (nm) **	32	28	25	23	20	18	16	14	13
Contact in resist (nm)	111	97	84	73	64	56	50	44	39
Contact after etch (nm)	101	88	77	67	58	51	45	40	36
*Gate CD control (3 sigma) (nm) [B] ***	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.3
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	90	78	68	59	52	45	40	36	32
Chip size (mm^2)									
Maximum exposure field height (mm)	26	26	26	26	26	26	26	26	26
Maximum exposure field length (mm)	33	33	33	33	33	33	33	33	33
Maximum field area printed by exposure tool (mm^2)	858	858	858	858	858	858	858	858	858
Number of mask levels MPU	33	33	33	35	35	35	35	35	35
Number of mask levels DRAM	24	24	24	24	24	26	26	26	26
Wafer size (diameter, mm)	300	300	300	300	300	300	300	450	450

** MPU physical gate length numbers and colors are determined by several working groups and the ORTC.*
*** Noted exception for RED in next three years: Solution NOT known, but does not prevent production manufacturing.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

2013 ITRS Roadmap

Table LITH1 Lithography Technology Requirements

Year of Production	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*	*2027*	*2028*
DRAM																
DRAM minimum ½ pitch (nm)	28	26	24	22	20	18	17	15	14	13	12	11	10.0	9.2	8.4	7.7
CD control (3 sigma) (nm) [B]	2.8	2.6	2.4	2.2	2.0	1.8	1.7	1.5	1.4	1.3	1.2	1.1	1.0	0.9	0.8	0.8
Minimum contact/via after etch (nm) [H]	28	26	24	22	20	18	17	15	14	13	11.9	10.9	10.0	9.2	8.4	7.7
Minimum contact/via pitch(nm)[H]	85	78	72	66	60	55	51	46	43	39	36	33	30	28	25	23
Overlay (3 sigma) (nm) [A]	5.7	5.2	4.8	4.4	4.0	3.7	3.4	3.1	2.8	2.6	2.4	2.2	2.0	1.8	1.7	1.5
k1 (13.5nm) EUVL	0.52	0.64	0.58	0.53	0.49	0.45	0.41	0.38	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Flash																
Flash ½ pitch (nm) (un-contacted poly)	18	17	15	14	13	12	12	12	12	12	12	12	12	12	12	12
CD control (3 sigma) (nm) [B]	1.8	1.7	1.5	1.4	1.3	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Contact CD after etch (nm) [G]	28	26	24	22	20	18	18	18	18	18	18	18	18	18	18	18
Overlay (3 sigma) (nm) [A]	6.1	5.6	5.1	4.7	4.3	3.9	3.9	3.9	3.9	3.9	3.9	3.9	3.9	3.9	3.9	3.9
k1 (13.5nm) EUVL	0.34	0.41	0.38	0.35	0.32	0.29	0.29	0.29	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
MPU/ Logic																
MPU/ASIC Minimum Metal ½ pitch (nm)	40	32	32	28	25	23	20	18	16	14.2	12.6	11.3	10.0	8.9	8.0	7.1
MPU/ASIC finFET fin minimum 1/2 pitch (nm)	30	24	24	21	19	17	15.0	13	12	10.6	9.5	8.4	7.5	6.7	6.0	5.3
MPU High-Performance Gate Length in resist (nm)	28	25	22	20	18	16	14	12	11	9.9	8.8	7.9	7.0	6.2	5.6	5.1
MPU High-Performance Physical Gate Length (nm)	20	18	17	15	14	13	12	11	9.7	8.9	8.1	7.4	6.7	6.2	5.6	5.1
*Gate CD control (3 sigma) (nm) [B] ***	2.0	1.8	1.7	1.5	1.4	1.3	1.2	1.1	1.0	0.9	0.8	0.7	0.7	0.6	0.6	0.5
MPU/ASIC minimum contact hole pitch (nm)	144	115	115	102	91	81	72	64	57	51	46	41	36	32	29	26
Contact/via after etch (nm) [H]	40	32	32	28	25	23	20	18	16	14	12.6	11.3	10.0	8.9	8.0	7.1
Overlay (3 sigma) (nm) [A]	8.0	6.4	6.4	5.7	5.1	4.5	4.0	3.6	3.2	2.8	2.5	2.3	2.0	1.8	1.6	1.4
k1 (13.5nm) EUVL	0.74	0.78	0.78	0.69	0.62	0.55	0.49	0.44	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Chip size (mm^2)																
Maximum exposure field height (nm) [E]	26	26	26	26	26	26	26	26	13	13	13	13	13	13	13	13
Maximum exposure field length (nm) [E]	33	33	33	33	33	33	33	33	16.5	16.5	16.5	16.5	16.5	16.5	16.5	16.5
Maximum field area printed by exposure tool (mm^2) [E]	858	858	858	858	858	858	858	858	214.5	214.5	214.5	214.5	214.5	214.5	214.5	214.5
Wafer site flatness at exposure step (nm) [C]	30	28	26	24	22	20	18	17	16	15	14.0	13.0	12.0	11.0	10.0	9.0
NA required for logic (single exposure)	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35
NA required for double exposure (Flash)	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35
NA required for double exposure (logic)	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35
EUV (13.5nm) NA [F]	0.25	0.33	0.33	0.33	0.33	0.33	0.33	0.33	>0.5	>0.5	>0.5	>0.5	>0.5	>0.5	>0.5	>0.5
minimum half pitch (DRAM, Flash, MPU metal, MPU fin) (nm)	18	17	15	14	13	12	12	11.9	11.9	10.6	9.5	8.4	7.5	6.7	6.0	5.3
minimum contact CD after etch (DRAM, MPU, Flash) (nm)	28	26	24	22	20	18	17	15	14	13	12	11	10.0	8.9	8.0	7.1
minimum CD control (DRAM, MPU, Flash) (3 sigma) (nm)	1.8	1.7	1.5	1.4	1.3	1.2	1.2	1.1	1.0	0.9	0.8	0.7	0.7	0.6	0.6	0.5
minimum required OL (DRAM, Flash, MPU) 3 sigma (nm)	5.7	5.2	4.8	4.4	4.0	3.7	3.4	3.1	2.8	2.6	2.4	2.2	2.0	1.8	1.6	1.4

Manufacturable solutions exist, and are being optimized

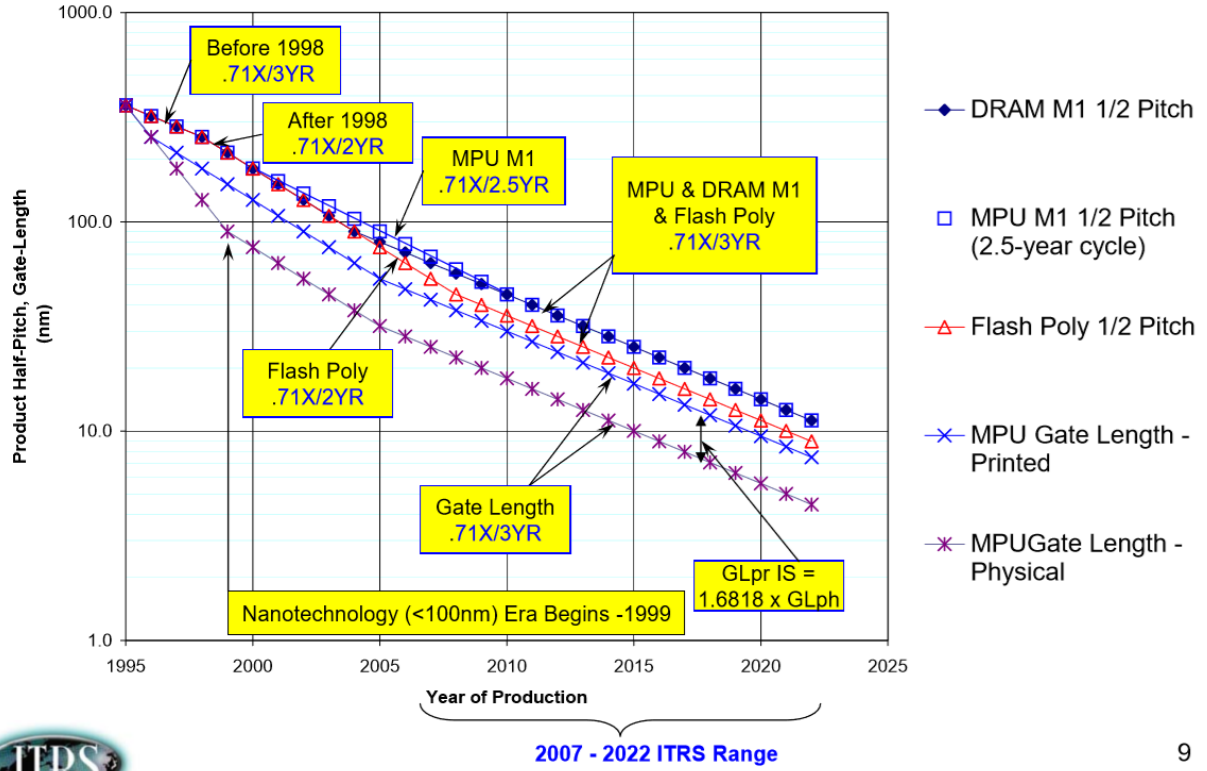
Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

2007 ITRS Product Technology Trends - Half-Pitch, Gate-Length

[WAS]



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